TEK

Part No. 070-4416-I
Product Group 26

494/494P
SPECTRUM ANALYZEI
OPTIONS INCLUDED
VOLUME 1

Part No. 070-4416-00
Product Group 26

494/494P
SPECTRUM ANALYZER
OPTIONS INCLUDED
VOLUME 1

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GENERAL INFORMATION

INTRODUCTION

The service instructions for this product consists of two volumes. Volume 1 contains the written information such as specifications, maintenance, and calibration. Volume 2 contains the diagrams and parts lists. Our intent is to provide both accurate and complete information for this product. The Table of Contents, at the beginning of this manual, lists the location and contents of each section that make up the two volume service manuals.

Change information that involves manual corrections and/or additions, pending manual reprint and bind, is located at the back of each service manual as a CHANGE INFORMATION section.

History

History information, with the updated data, is integrated into the text or diagrams. When a page is updated, the revised pages are identified by a revision date in the lower inside corner of the page. When a diagram is updated, the revision date is placed at the lower center of the diagram. History information is indicated with a gray tint. When a component value is changed, the designator on the drawing is boxed with a grey outline. When a circuit is deleted or changed, the original configuration is shown in grey, drawn either at its original location or to the side of the drawing. If you have a manual other than the one that came with your instrument it may contain revisions that do not apply to your instrument; however all history information that pertains to the earlier instruments is retained.

When a major modification has been made to an assembly or circuit board, the data for the replaced assembly will follow the new information and will be identified with appropriate titles or headings; such as instrument serial number range, or the assembly or board part numbers.

Level of Competence

It is assumed that whoever uses these instructions is familiar with basic digital, analog, and RF circuitry. Circuit analysis is mostly functional and should provide the technician with the information necessary to isolate the majority of malfunctions to a board or block of circuitry. The technician should then be able, with the aid of test equipment, to isolate the malfunction to a specific component or components.

This instrument contains internal firmware which provides a complete instrument check during power up and during operation, and if needed, guides the user through a front panel calibration procedure. If calibration cannot be achieved, a diagnostic test detects and isolates most problems to the system, such as 1st LO. The technician can then run trouble shooting diagnostic to further isolate the problem to the board or in some cases to the IC level. Refer to the Diagnostic part of the Maintenance section.

Standards and Conventions Used

Most terminology is in accordance with those standards adapted by IEEE and IEC. A glossary of terms is provided as an appendix. Abbreviations in the documentation are in accordance with ANSI Y1.1-1972, with exceptions and additions explained in parentheses after the abbreviation. Graphic symbols comply with ANSI Y32.2-1975. Logic symbology is based on ANSI Y32.14-1973 and the manufacturer's data description. GPIB functions for the programmable version conforms to IEEE 488-1978 Standard. A copy of ANSI and IEEE standards may be obtained from, the Institute of Electrical and Electronic Engineers Inc., 345 East 47th Street, New York, N.Y. 10017.

Conformance to Industry Standards

The 494/494P complies with the following Industry Safety Standards and Regulatory Requirements:

Safety.

CSA—Electrical Bulletin

FM—Electrical Utilization Standard Class 3820
ANSI C39.5—Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation.
IEC 348 (2nd addition)—Safety Requirements for Electronic Measuring Apparatus.

Regulatory Requirements

VDE 0871 Class B—Regulations for RFI Suppression of High Frequency Apparatus and Installations.

Product Description

The 494 and the 494P programmable instruments are high performance, compact, portable spectrum analyzers. Microcomputer control of most functions simplifies and enhances operation. Its features synthesizer frequency accuracy and stability, precision signal counting ability, precise amplitude measurement capability, digital storage display, battery-powered memory to retain front panel settings and displays, and crt message readout that describes function of the front panel controls and selectors along with messages that explain operating errors. Some of the options provide a second language for display messages, waveguide mixers to extend the frequency range to 325 GHz, rackmount and benchtop versions, and enhanced measurement capability for digital microwave radio.

The frequency range is 10 kHz to 21 GHz with the internal mixer, and up to 325 GHz when using external waveguide mixers. A minimum resolution bandwidth of 30 Hz, with a minimum span of 50 Hz/div, provides measurement resolution that is commmensurate with the frequency accuracy. Digital storage provides flicker free displays plus functions such as SAVE A, B – SAVE A, MAX HOLD with which to compare and subtract displays, save maximum values. In addition to the conventional digital storage feature, up to nine separate displays with their parameter readouts, can be stored in battery-powered memory, then later recalled for additional analysis and comparison. Up to ten different front-panel control setups can also be stored for future recall.

Center frequency may be selected by means of the front-panel tuning knob or directly entered via the Data Entry keyboard. When using the keyboard, it is not necessary to alter the Span/Div setting regardless of the frequency selected. Other parameters, such as vertical display and reference level, may also be keyboard selected with the flexibility previously available only under GPIB program control. Counter accuracy to 1 Hz resolution is available.

In addition, the 494/494P requires only a short warm-up time for stable operation. In 15 minutes or less, the frequency drift is less than 500 Hz per minute of sweep time. After one hour, it is less than 50 Hz per minute of sweep time. Display dynamic range is 80 dB, with calibrated reference level readout from −117 dBm to +30 dBm, in selectable steps from 1 to 15 dB, and 0.25 dB for a Δ A (amplitude) mode. When the vertical display is selected with the Data Entry keyboard, the reference level steps correspond to the display mode (see Operating instructions). Sensitivity at 30 Hz resolution bandwidth is −121 dBm to 7.1 GHz, decreasing to −96 dBm at 21 GHz.

The 494P adds remote control capability to the standard instrument features of the 494. The front-panel controls (except those intended for local use, such as INTENSITY) can be remotely operated through the GPIB port, which allows the 494P to be used with a variety of systems and controllers. This operation is described in detail in the Programmers manual.

Product Service

To assure adequate product service and maintenance for our instruments, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available. For example; for a fixed fee, a maintenance agreement program provides maintenance and re calibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time. Contact your local Service Center, representative, or sales engineer for details regarding: Warranty, Calibration, Emergency Repair, Repair Parts, Scheduled Maintenance, Maintenance Agreements, Pickup and Delivery, On-Site Service for fixed installations, and other services available through these centers.

Tektronix emergency repair service provides immediate attention to instrument malfunctions if you are in an emergency situation such as a field trip. Again, contact any Tektronix Service Center for assistance to get you on your way within a minimum of time.

Instrument Construction

The modular construction of the 494/494P instrument provides ready access to the major circuits. Circuit boards that contain sensitive circuits are either mounted on metal extrusions, each of which provides shielding between adjacent modules, or they are mounted within honeycomb-like extrusions, with feedthrough connectors through the wall of the compartment. All boards and assemblies plug onto a common mother board which provides the interconnection for these boards and assemblies. Most adjustments and test points are accessible while the instrument is operational and the modules or assemblies secured in their normal position. Extenders are provided with an optional Service Kit (see Maintenance section under Service Fixtures and Tools for Maintenance).

Any module or board can be removed without disturbing the structural or functional integrity of the other modules. The extenders allow most circuit board assemblies to function in an extended position for service or adjustment. The circuit boards mounted on the metal extrusion can be removed by removing the securing screws. All other circuit boards (which should require minimal service) are accessible by removing a cover plate over the assembly or module.

NOTE

Disassembly of some modules may require special tools and procedures. These procedures will be found in the Maintenance section.

To obtain and maintain the frequency stability, sensitivity, and EMI characteristics, circuits are completely RF isolated to ensure spurious free response; yet the close proximity minimizes losses or interactions with other functions. All compartments are enclosed on both sides by metal plates and all interconnections between compartments are made by feedthrough terminals rather than cables. If the compartments are opened, be sure that the shields and covers are properly reinstalled before operating.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments, is installed on the Z Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time. Most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Installation, Preparation for Use, and Repackaging

This section provides unpacking information and the procedures to prepare the instrument for use. It also includes repackaging information.

Changing Power Input Range

The procedure for changing the input voltage range is described under the Installation and Repackaging section.

The power cord that is supplied with the instrument and the instrument power voltage requirements depend on the available power source (see Specification section). Power cord options are described in the Installation and Preparation for Use section and the Options section.

Standard Accessories

Standard accessories for the 494/494P and rackmount/benchtop versions are listed in Table 1-1 and in Volume 2 of the Service Instructions, following the Replaceable Mechanical Parts list. The list in Volume 2 of the Service instructions provides part numbers for these accessories.

Options

Options for the 494/494P are described in the Options section of the manuals including rackmount/benchtop versions.

Optional Accessories

Optional accessories that play a significant role in the full operational applications and servicing of the 494/494P are referenced, where appropriate, throughout these instructions as well as the operating instructions.

Selected Components

Some components, such as microcircuits, are selected to meet Tektronix specifications. These components are indicated in the parts list and carry a Tektronix Part Number under the Mfr. Part Number column.

Selected value components that compensate for parameter differences between active components are identified on the circuit diagram and in the parts list as a "SEL" value. The component description lists either the nominal value or a range of value. If the procedure for selection is not obvious, such as setting the gain or response of a stage, the criteria for selection is explained in the Adjustment or Maintenance section of the manual.

Component Circuit Numbering Scheme

In this instrument, circuit numbers were assigned according to the physical location of the component on the board. For example, a resistor, located within row 2 column 08, is R2080. The fourth digit of the number is an expander used to designate two or more common components within a given grid, such as R2080, R2082, etc. Chassis mounted components are assigned a three digit number. This identifies these components from the board mounted components.

The Replaceable Electrical Parts list prefixes these circuit numbers with an assembly number. R2080 on assembly A20 becomes A20R2080. Assembly and subassembly numbers are assigned in numerical order by location within the instrument.

Firmware Version and Error Message Readout

This feature of the 492/492P provides readout of the firmware version when the power on/off is cycled. During initial power-up cycle, the firmware version flashes on screen for approximately two seconds. The Replaceable Electrical Parts list section, under Memory Board (A54), lists the ROM's and their Tektronix part number for each firmware version.

An additional feature is error message readout. When a routine fails, a message comes on screen describing the error and what can be done to bypass the problem if it can not be corrected.

Rackmount/Benchtop Versions

A rackmount version of the 492/492P Spectrum Analyzer is available to install the instrument in a standard 19 inch rack. The benchtop version is the same as the rackmount with the exception of the side rails. Complete information can be found in the Options section of this manual.

Replacing Fuses

Refer to the Installation and Preparation for Use section for line fuse replacement and the Maintenance section for replacing the power supply fuses.

Options For Power Cord Configuration

Tektronix has implemented options that provide internationally approved power cord and plug configurations. These are illustrated and described in Installation and Preparation for Use section and the Options section.

Table 1-1
STANDARD ACCESSORIES

Nomenclature	Qty.	Storage
50 Ω coax cable, N to N connector, 6 ft	1	Cover or Drawer
50 Ω coax cable, bnc to bnc connector, 18 inches	1	Cover or Drawer
Visor Crt	1	
Manual, Operators Handbook	1	Cover or Drawer
Manual, Operators	1	
Manual, Service Vol. 1	1	
Manual, Service Vol. 2	1	
Manual, Programmers (494P only)	1	
Adapter, N male to bnc female	1	Cover or Drawer
[a]Fuses, 4A, Fast	2	Cover or Drawer
[a]Power cord	1	
Cord clamp	1	
Crt Light Filter, Amber	1	Cover or Drawer
Crt Light Filter, Gray	1	Cover or Drawer
Crt Mesh Filter	1	Cover or Drawer
[b]Diplexer Assembly	1	Cover or Drawer
1-Adapter, TNC to SMA	1	(Part of Diplexer Assembly)
1-Cable, semi-rigid coax	1	(Part of Diplexer Assembly)
Cable, GPIB Interconnect (494P only)	1	

[a] The power cord (161-0104-00) and fuses are replaced with an appropriate power cord, for the international power cord options (A1, A2, A3, A4, and A5) and the fuses are replaced with 2A slow blow.

Option 52 (North American configuration for 220 V with standard power cord) also replaces fuses with 2A slow blow.

[b]Deleted with Option 08

SPECIFICATION

Introduction

This section includes electrical, physical, environmental, and safety characteristics of this instrument. Changes to this specification, due to options are listed in the Options section.

ELECTRICAL CHARACTERISTICS

The following tables of electrical characteristics and features apply to the 494/494P Spectrum Analyzer after a 30-minute warmup, except as noted. The Performance Requirement column defines some characteristics in quanitative terms and in limit form. The Supplemental column explains performance requirements or provides performance information. Statements in this column are not considered to be guaranteed performance and are not ordinarily supported by a performance check procedure. Procedure to verify performance requirements are provided in the Performance section of the service manual.

The instrument microprocessor performs an internal calibration check each time power is turned on and verifies that the instrument frequency and amplitude performance is as specified. An operation or functional check procedure, which does not require external test equipment or technical expertise, is provided in the operators instructions to satisfy most incoming inspections and help familiarize the operator with the capabilities of the instrument.

Verification of Tolerance Values

Compliance tests of specified limits, listed in the Performance Requirement column, shall be performed after sufficient warmup time and preliminary preparation (such as front panel adjustments). Measurement shall be made by instruments that do not affect the values measured. Measurement tolerance of test equipment should be negligible in comparison to the specified tolerance and when not negligible, the error of the measuring device shall be added to the tolerance specified.

Table 2-1
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Center Frequency Range (internal mixer)		10 kHz to 21 GHz. Tuned by the front panel knob or front panel Data Entry keyboard.
Accuracy (after the front panel CAL has been performed)		Accuracy of the center frequency is a function of the accuracy to which the center frequency is set between sweeps (covered by CF accuracy specification), and the amount of center frequency drift during a sweep. Center frequency drift can be significant during the first 30 min. after turn-on, or after a change in ambient temperature.
Bands 1 & 5-12 with Span/Div >200 kHz, and Bands 2-4, with Span/Div >100 kHz	±[(20% of Span/Div or Resoln Bandwidth, whichever is greater) + (CF × ref freq error) + (N × 15 kHz)]	Refer to "IF Frequency, LO Range, and Harmonic Number" specification for value of N. The 1st LO is unlocked in these spans. When the center frequency is changed within a band, a settling time of 1 s/GHz change in center frequency, divided by N should be allowed.
Bands 1 & 5-12 with Span/Div ≤200 kHz and bands 2-4 with Span/Div ≤100 kHz	±[(20% of Span/Div or Resoln Bandwidth, whichever is greater) + (CF × ref freq error) + (2N + 25 Hz)]	The 1st LO is phase locked in these spans

Table 2-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
CF Drift (constant ambient temperature and fixed center frequncy) After 30 minute warmup: Bands 1 & 5-12 with Span/Div >200 kHz, and Bands 2-4 with Span/Div >100 kHz		Since the center frequency is corrected before each sweep the only error observed is during sweep time. ≤(25 kHz)N per minute of sweep time
Bands 1 & 5-12 with Span/Div ≤200 kHz Bands 2-4 with Span/Div ≤100 kHz		≤150 Hz per minute of sweep time
After 1 hour warmup: Bands 1 & 5-12 with Span/Div >200 kHz and Bands 2-4 with Span/Div >100 kHz		≤(5 kHz) N per minute of sweep time
Bands 1 & 5-12 with Span/Div ≤200 kHz and Bands 2-4 with Span/Div ≤100 kHz	≤50 Hz per minute of sweep time	
Readout Resolution		At least 10% of Span/Div
Signal Counter Accuracy	±[(Counter frequency × frequency reference error) + (10 + 2N)Hz + 1 LSD]	
Sensitivity	Signal level at center screen must 20 dB or more above the average noise level and within 60 dB of the Reference Level	
Readout Resolution		1 Hz through 1 GHz, selectable with COUNT RESOLN control
Reference Frequency Error Aging Rate		1×10^{-7} for first six months then less than 1×10^{-7} per year
Accuracy during warmup at 25°C (ambient) and 30 minutes after power on		Within 5×10^{-8} of the frequency after 24 hours
Temperature sensitivity		Within 2×10^{-8} over the instrument operating range of −15°C to +55°C, referenced to +25°C
Residual FM (short term) after 1 hour warmup: Bands 1 & 5-12 with Span/Div >200 kHz, and bands 2-4 with Span/Div >100 kHz	≤(7 kHz)N total excursion in 20 ms	
Bands 1 & 5-12 with Span/Div ≤200 kHz Bands 2-4 with Span/Div ≤100 kHz	≤(10+2N)Hz total excursion in 20 ms	

Table 2-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
"Static" Resolution Bandwidth (6 dB down)	30 Hz then 100 Hz to 1 MHz in decade steps plus an AUTO position. Resolution bandwidth is within 20% of the selected bandwidth.	In AUTO position the bandwidth is automatically selected by an internal computer whose output depends on the setting of the SPAN/DIV, TIME/DIV, Vertical Display, and Video Filter selectors. When the RESOLUTION BANDWIDTH and TIME/DIV selectors are set to AUTO the microcomputer selects the optimum resolution for the SPAN/DIV settings.
Shape Factor (60 dB/6 dB)	7.5:1 or less, and 15:1 or less for 30 Hz resolution bandwidth.	
Noise Sidebands	At least −75 dBc at 30 times the resolution offset (−70 dBc for resolution bandwidths ≤100 Hz).	
Video Filter Narrow		Reduces video bandwidth to approximately 1/300 of the selected resolution bandwidth and 1/100 for 30 Hz bandwidth.
Wide		Reduces video bandwidth to approximately 1/30 of the selected resolution bandwidth and 1/10 for 30 Hz bandwidth.
Pulse Stretcher Fall-time		30 μs/div (±50%)
Frequency Span/Div Range—in a 1-2-5 sequence with the SPAN/DIV control, or by two significant digits from the Data Entry keyboard		**Band** / **Narrow Span/Div** / **Wide Span/Div** 1-3 (0-7.1 GHz) / 50 Hz / 200 MHz 4-5 (5.4-21 GHz) / 50 Hz / 500 MHz 6 (18-26 GHz) / 50 Hz / 1 GHz 7-9 (26-90 GHz) / 50 Hz / 2 GHz 10 (75-140 GHz / 50 Hz / 5 GHz 11-12 (110-325 GHz) / 50 Hz / 10 GHz Two additional positions provide full band (MAX Span) display or 0 Hz (Zero Span) display.
Accuracy/Linearity	Within 5%, of the selected Span/Div over the center 8 divisions of a 10 division display.	

Table 2-1 (cont)

Characteristic	Performance Requirement		Supplemental Information
[a]Frequency Response Coaxial (direct) Input	**About the mid-point (mean) between two extremes**	**Referenced to 100 MHz**	Frequency response is measured with 10 dB of RF attenuation and Peaking optimized for each center frequency setting, when applicable. Response includes the effect of input vswr, mixing mode (N), gain variation, pre-selector, and mixer. Digital storage typically increases errors by ±0.5%. Display flatness is typically 1 dB greater than frequency response. Refer to Rackmount/Benchtop data (Option 30, 31, and 32) in the Options section for variance.
Band 1 50 kHz-1.8 GHz 10 kHz-1.8 GHz	±1.5 dB ±2.0	±2.5 dB ±3.0 dB	
Band 2 1.7-5.5 GHz	±2.5 dB	±3.5 dB	
Band 3 3.0-7.1 GHz	±2.5 dB	±3.5 dB	
Band 4 5.4-18.0 GHz	±3.5 dB	±4.5 dB	
Band 5 15.0-21.0 GHz	±5.0 dB	±6.5 dB	
External Tektronix High Performance Waveguide Mixers			
Band 6 18.0-26 GHz	±3.0 dB	±6.0 dB	
Band 7 26.0-40.0 GHz	±3.0 dB	±6.0 dB	
Band 8 33.0-60.0 GHz	±3.0 dB	±6.0 dB	
Band 9 50.0-90.0 GHz			Typically ±3 dB over any 5 GHz bandwidth
Band 10 75.0-140.0 GHz			Typically ±3 dB over any 5 GHz bandwidth
Band 11 110-220 GHz			Typically ±3 dB over any 5 GHz bandwidth
Band 12 170-325 GHz			Typically ±3 dB over any 5 GHz bandwidth

[a]Refer to "Verification of Tolerance Limits" at the beginning of this specification.

Table 2-2
IF Frequency, LO Range, and Harmonic Number (N)

Band and Freq Range		LO Range and Harmonic (N)	1st IF (MHz)
1 (0—1.8 GHz)		2072-3872 (1−)	2072
2 (1.7—5.5 GHz)		2529-6329 (1−)	829
3 (3.0—7.1 GHz)		2171-6271 (1+)	829
4 (5.4—18.0 GHz)		2072-6276 (3−)	829
5 (15—21 GHz)		4309-6309 (3+)	2072
6 (18—26 GHz)		2655-4071 (6+)	2072
7 (26—40 GHz)		2443-3793 (10+)	2072
8 (33—60 GHz)		3792-5790 (10+)	2072
9 (50—90 GHz)		3195-5862 (15+)	2072
10 (75—140 GHz)		3170-6000 (23+)	2072
11 (110—220 GHz)		2917-5790 (37+)	2072
12 (170—325 GHz)		2998-5841 (56+)	2072

Table 2-3
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Vertical Display Modes		10 dB/Div, 2 dB/Div, and linear. Any integer between 1-15 dB/Div can also be selected with the Data Entry keyboard.
Reference Level (full screen) Range		−117 dBm to +40 dBm; +40 dBm includes 10 dB of IF gain reduction, +30 dBm is the maximum safe input for log mode. In LIN mode, range is 50 nV/Div to 2 V/Div, 1 W maximum safe input
Steps		In the 10 dB/DIV display mode, steps are 10 dB for the coarse mode and 1 dB for the FINE mode. In the 2 dB/DIV mode, steps are 1 dB for coarse and 0.25 dB for FINE. When the dB/Div is set through the Data Entry keyboard, the coarse steps correspond to the display mode. The FINE steps are 1 dB when the mode is 5 dB/Div or more and 0.25 dB/Div for display modes of 4 dB/Div or less (referred to as ΔA mode). In LIN mode the steps are in equivalent 1 dB increments for FINE and in a 1-2-5 Volts/Div sequence for coarse.

Table 2-3 (cont)

Characteristic	Performance Requirement	Supplemental Information
Accuracy		Accuracy is a function of RF attenuation, IF gain, resolution bandwidth, display mode, calibrating source (i.e., internal calibrator), frequency band and response. Refer to accuracies of these characteristics. When the CAL button is activated the processor runs a calibrating routine, which if completed, reduces the REF LEVEL error between different resolution bandwidths. Also, if the instrument ambient temperature is changed after a calibration is run, the REF LEVEL error typically can change ±0.05 dB/°C but may increase to ±0.15 dB/°C with some instrument settings. The input RF attenuator steps 10 dB for reference level changes above −30 dBm (−20 dBm when MIN MOISE is active) unless the MIN RF ATTEN setting is greater than zero. The IF gain increases 10 dB for each 10 dB reference level change below −30 dBm (−20 dBm for MIN NOISE mode).
Display Dynamic Range		80 dB maximum, for log mode, and 8 divisions linear
Accuracy	±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over 80 dB range ±0.4 dB/2 dB to a maximum cumulative error of ±1.0 dB over 16 dB range LIN mode is ±5% of full scale	
RF Attenuator Range		0-60 dB in 10 dB steps
Accuracy [a]Dc to 4 GHz	Within 0.3 dB/10 dB to a maximum of 0.7 dB over the 60 dB range	
4 GHz to 18 GHz	Within 0.5 dB/10 dB to a maximum of 1.4 dB over the 60 dB range	
IF Gain Range		87 dB of gain increase, 10 dB of gain decrease (MIN NOISE activated), in 10 dB and 1 dB steps.
Accuracy	Gain steps are monotonic (same direction) with the following limits: Within 0.2 dB/dB to a maximum of 0.5 dB/9 dB, except at the decade transistions of −19 to −20 dBm, −29 to −30 dBm, −39 to −40 dBm, −49 to −50 dBm, and −59 to −60 dBm; where an additional 0.5 dB can occur, for a total of 1.0 dB per decade. Maximum deviation over the 97 dB range is within ±2 dB.	

Table 2-3 (cont)

Characteristic	Performance Requirement	Supplemental Information
Gain Variation between Resolution Bandwidths; (after CAL routine has been run)		Measured at −20 dBm MIN DISTORTION mode
With respect to 1 MHz filter	Less than ±0.4 dB	
Between any two filters	Less than 0.8 dB	
Differential Amplitude Measurement		ΔA mode provides differential measurements in 0.25 dB increments.
Range		0 dB above to 48 dB below the reference level established when the ΔA mode was activated. DO NOT USE ΔA mode above +30 dBm reference level.
Accuracy		**dB Difference** / **Steps** / **Error**: 0.25 / 1 / 0.15 dB; 2 / 8 / 0.4 dB; 10 / 40 / 1.0 dB; 50 / 200 / 2.0 dB
Spurious Responses Residual (no input signal), referenced to mixer input, and fundamental mixing for bands 1-3.	−100 dBm or less	
Intermodulation products 50 kHz to 1.8 GHz (Band 1 and 1.8 to 21.0 GHz for Bands 2-4)	At least −70 dBc from any two on screen signals within any frequency span	≥−100 dBc when signals are separated 100 MHz or more in preselected bands
1.7-1.8 GHz (Band 2 only)	At least −70 dBc from any two −40 dBm signals within any frequency span	
Harmonic Distortion 50 kHz-1.8 GHz (Band 1)	At least −60 dBc below a full screen signal in MIN DISTORTION mode	
1.7-21 GHz	At least −100 dBc	
LO Emission, with no (0) RF attenuation	Less than −70 dBm to 21 GHz	

[a]Refer to "Verification of Tolerance Limits" at the beginning of this specification.

Table 2-4
SENSITIVITY

Equivalent maximum input noise for each resolution bandwidth, using the internal mixer for bands 1–5 (50 kHz–18 GHz), and Tektronix High Performance Waveguide Mixers for bands 6–12 (18–325 GHz).

Band/Frequency	Equivalent Input Noise in dBm versus Resolution Bandwidth					
	30 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
Band 1 50 kHz-1.8 GHz	−121	−118	−110	−100	−90	−80
Bands 2 & 3 1.7-7.1 GHz	−121	−118	−110	−100	−90	−80
Band 4 5.4-12.0 GHz	−106	−103	−95	−85	−75	−65
Band 4 12.0-18.0 GHz	−101	−98	−90	−80	−70	−60
Band 5 15.0-21.0 GHz	−96	−93	−85	−75	−65	−55
[a]Band 6 18.0-26.5 GHz	−111	−108	−100	−90	−80	−70
[a]Band 7 26.5-40.0 GHz	−106	−103	−95	−85	−75	−65
[a]Band 8 33.0-60.0 GHz	−106	−103	−95	−85	−75	−65
[a]Band 9 50.0-90.0 GHz	Typically −95 dBm for 1 kHz bandwidth at 50 GHz, degrading to −85 dBm at 90 GHz					
[a]Band 10 75.0-140 GHz	Typically −90 dBm for 1 kHz bandwidth at 75 GHz, degrading to −75 dBm at 140 GHz					
[a]Band 11 110-220 GHz	Typically −80 dBm for 1 kHz resolution bandwidth at 110 GHz, degrading to −65 dBm at 220 GHz					
[a]Band 12 170-325 GHz	Typically −70 dBm for 1 kHz resolution bandwidth at 170 GHz, degrading to −55 dBm at 325 GHz					

[a]Tektronix High Performance Waveguide Mixers

Table 2-5
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
RF INPUT		Type N female connector, specified to 21 GHz.
Input Impedance		50 Ω; vswr with RF attenuation ≥10 dB: 50 kHz-2.5 GHz: 1.3:1 (typically 1.2:1) 2.5-6.0 GHz; 1.7:1 (typically 1.5:1) 6.0-18 GHz; 2.3:1 (typically 1.9:1) 18-21 GHz; 3.5:1 (typically 2.7:1)
Maximum Safe Input		+30 dBm (1 W) continuous, 75 W peak, pulse width 1 μs or less with a maximum duty factor of 0.001 (attenuator limit). DO NOT APPLY DC VOLTAGE TO THE RF INPUT
1 dB Compression Point (minumum) 1.7-2.0 GHz	−28 dBm	With no RF attenuation
Otherwise	−18 dBm	With no RF attenuation
Optimum level for linear operation		−30 dBm, referenced to input mixer. This is achieved in MIN DISTORTION mode when not exceeding full screen display.
External Mixer		Input for an IF signal and the source of bias for external waveguide mixers. Bias range +1.0 to −2.0 V, 70 Ω source.
EXTERNAL REFERENCE Frequency	1, 2, 5, or 10 MHz, ±5 ppm	
Power	−15 dBm to +15 dBm.	
Waveshape		Sinewave, ECL or TTL. (Allowable duty cycle symmetry is 40-60%)
Input Impedance		50 Ω ac, 500 Ω dc
HORIZ/TRIG		Dc coupled input for horizontal drive and ac coupled for trigger signal
Input Voltage Range Sweep		0 to −10 V (dc + peak ac) for full screen deflection
Trigger	1.0 V peak, frequency 15 Hz to 1 MHz	Maximum input: 50 V (dc + peak ac). Maximum ac input: 30 Vrms to 10 kHz then derate linearly to 3.5 Vrms at 100 kHz and above. Pulse width is 0.1 μs minimum.
MARKER/VIDEO		Video, 0 to +4 V, if Ext Video is selected; or, it interfaces with the 1405 TV Sideband Adapter to insert an externally generated marker on internal video. Marker 0 to −10 V
ACCESSORY (J104) Pin 1—External Video Select		TTL logic 0 selects the External Video Input
Pin 2—External Preselector Out		±15 V maximum
Pin 3—External Preselector Return		
Pin 5—Chassis Gnd		

Table 2-6
OUTPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Calibrator (CAL OUT)	−20 dBm ± 0.3 dB at 100 MHz (phase locked to reference oscillator)	100 MHz comb of markers provide amplitude calibration at 100 MHz and markers for frequency and span calibration, to 1.0 GHz
1st LO and 2nd LO		Provides access to the output of the respective local oscillators. 1st LO +7.5 dBm minimum, to a maximum of +15 dBm; 2nd LO −22 dBm minimum, to a maximum of +15 dBm. THESE PORTS MUST BE TERMINATED IN 50 Ω AT ALL TIMES.
EXTERNAL MIXER		In the EXTERNAL MIXER mode, bias range is +1.0 to −2.0 V; or, with change of internal straps, −1.0 to +2.0 V.
VERTical		Provides 0.5 V ±5% of signal per division of video that is above and below the centerline. Source impedance approximately 1 kΩ.
HORIZ Out		Provides 0.5 V/div either side of center. Full range −2.5 V to +2.5 V. Source impedance approximately 1 kΩ.
PEN LIFT		TTL compatible, nominal +5 volts to lift pen.
10 MHz IF		Access to the 10 MHz IF. Output level is approximately −5 dBm for a full screen signal at −30 dBm reference level. Nominal impedance approximately 50 Ω.

Table 2-7
GENERAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
IEEE Std 488-1978 Port (GPIB) 494P		In accordance with IEEE 488 standard, and Tektronix codes and format standard Version 81.1
PROBE POWER		Provides operating voltages for active probes. Output voltages are: Pin 1, +5 V @ 100 mA max. Pin 2, ground. Pin 3, −15 V @ 100 mA max. Pin 4, +15 V @ 100 mA max. (see Figure 2-1)
Sweep Sweep Time	20 μs/Div to 5 s/Div in 1-2-5 sequence (10 s/Div available in AUTO).	Triggered, auto, manual, and external.
Accuracy	±5%.	
Triggering	2 division or more of signal for internal; and 1.0 V peak, minimum, for external	
Crt Readout		Displays: Reference level, frequency, vertical display mode, frequency span/div, frequency range, resolution bandwidth, RF attenuation, internal or external frequency reference, and GPIB states (494P only)
Non-volatile Memory		Instrument settings, displays, calibration offsets, and preselector peaking codes for each band are stored in back-up battery powered CMOS RAM. Battery life @ +55°C instrument ambient temperature, is 1-2 years. At +25°C, life should be greater than 5 years. Retention of data in non-volatile memory will occur over the range of −15°C to +55°C operating, and −30 to +85°C non-operating.

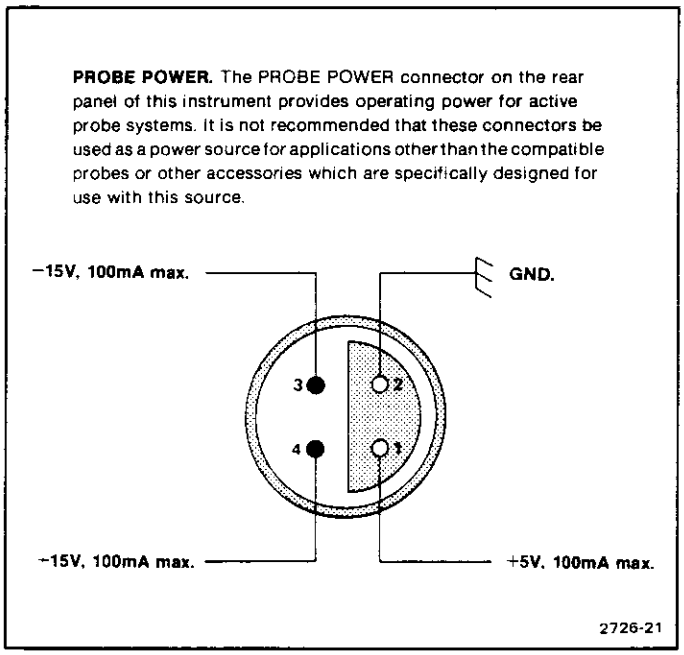


Figure 2-1. Probe Power connector pin out.

Table 2-8
POWER REQUIREMENTS

Characteristic	Description
Input Voltage	90 to 132 Vac or 180 to 250 Vac, 48 to 440 Hz.
Power	
Power	At 115 V, 60 Hz; 210 watts maximum, 3.2 amperes.
Leakage Current	5 mA maximum

NOTE

If power to this instrument is interrupted, it may be necessary to re-initialize the microcomputer; when power is restored, turn the POWER switch OFF for 5 seconds then back ON.

Table 2-9
ENVIRONMENTAL CHARACTERISTICS

Meets MIL T-28800C, type III class 3, style C specifications, comprised of the following:

Characteristic	Description
Temperature	
Operating and Humidity	−10 to +55°C/95% (+5%, −0%) relative humidity. (Instrument is tested and meets −15 to +55°C)
Non-operating	−62 to +85°C.

Table 2-9 (cont)

Characteristic	Description	
NOTE *After storage at temperatures below the operating range, the microcomputer may not initialize on power-up. If so, allow the instrument to warm up for 15 minutes and re-initialize the microcomputer by turning the POWER Off for 5 seconds then back On.*		
Altitude		
Operating	15,000 feet	
Non-operating	40,000 feet	
Humidity (Non-operating)	Five cycles (120 hours) in accordance with Mil-Std-810	
Vibration		
Operating (instrument secured to a vibration platform during test)	MIL-Std-810,Method 514 Procedure X (modified). Resonant searches along all three axis at 0.020 inch displacement, frequency varied from 5-55 Hz for 15 minutes. All major resonances must be minimum/axis plus dwell at the resonant frequency, or 55 Hz if no resonance is found for 10 minutes minimum. Total vibration time about 75 minutes.	
Shock (operating and non-operating)	Three shocks of 30 g, one-half sine, 11 ms duration each direction along each major axis. Guillotine-type shocks. Total of 18 shocks.	
Transit drop (free fall)	8 inch, one per each of six faces and eight corners. (Instrument is tested and meets drop height of 12 inches.)	
Electromagnetic Interference (EMI)	Meets requirements described in Mil-Std-461B Part 4, except as noted	
	Test Method	**Remarks**
Conducted Emissions	CEO1—60 Hz to 15 kHz.	1 kHz to 15 kHz only.
	CEO3—15 kHz to 50 MHz power leads.	15 kHz to 50 kHz, relaxed by 15 dB.
Conducted Susceptibility	CSO1—30 Hz to 50 kHz power leads.	Full limits.
	CSO2—50 kHz to 400 MHz power leads.	Full limits.
	CSO6—spike power leads.	Full limits.
Radiated Emissions	REO1—30 Hz to 50 kHz magnetic field.	Relaxed by 10 dB for fundamental to 10th harmonic of power line. Exceptioned, 30 kHz to 36 kHz.
	REO2—14 kHz to 10 GHz.	Full limit.
Radiated Susceptibility	RSO1—30 Hz to 50 kHz.	Full limit.
	RSO2—Magnetic Induction	To 5 A only
	RSO3—14 kHz to 10 GHz	Up to 1 GHz

Table 2-10
PHYSICAL CHARACTERISTICS

Characteristic	Description
Weight (standard accessories and cover, except manuals)	52 pounds (24 kg) maximum
Dimensions	
Without front cover, handle, or feet	6.9 X 12.87 X 19.65 inches (175 X 327 X 499 millimeters)
With front cover, feet, and handle	9.15 X 15.05 X 23.1 inches (232 X 382 X 587 millimeters) with the handle folded back over the instrument, 28.85 inches (732.8 mm) with the handled fully extended

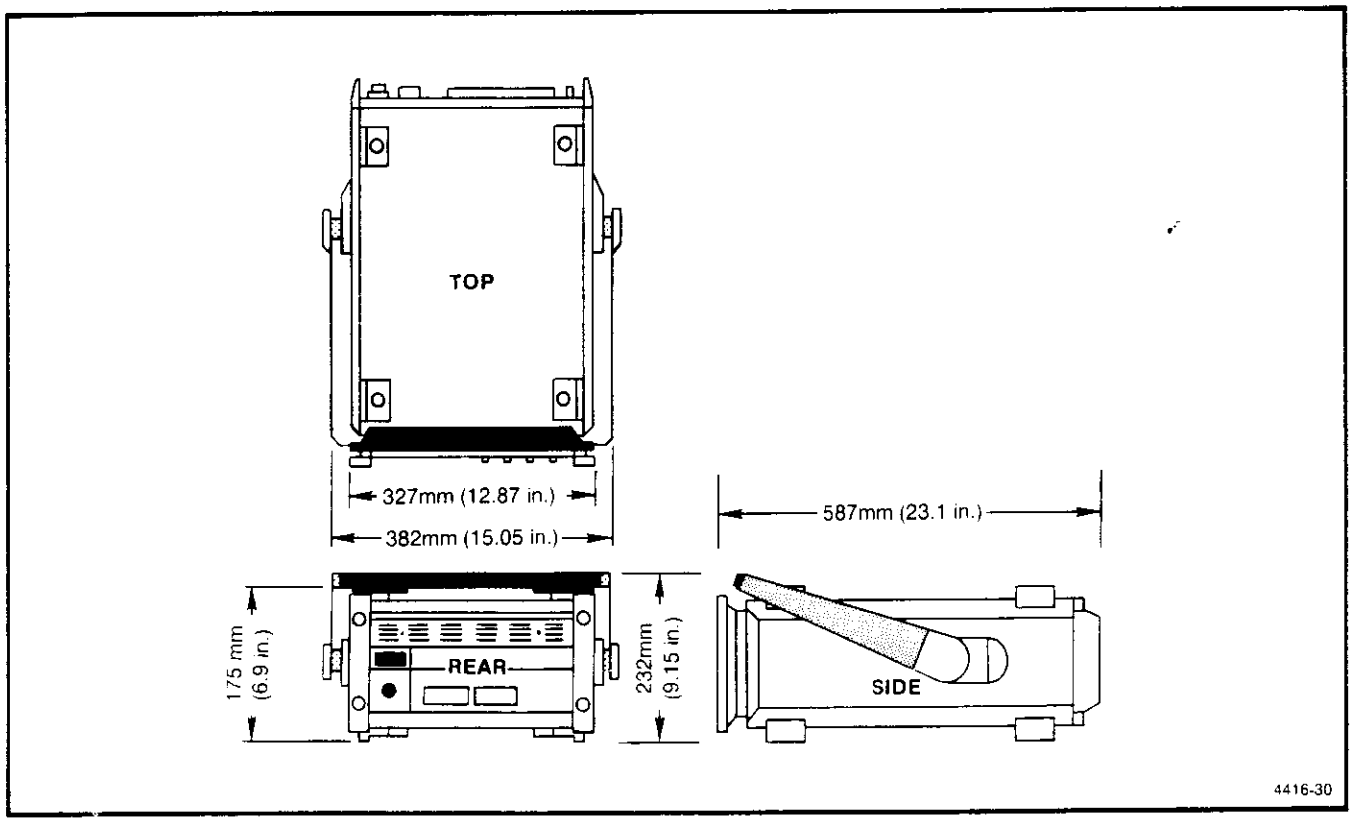


Figure 2-2. 494/494P Dimensions.

Table 2-11
494/494P SAFETY STANDARD AND REGULATORY REQUIREMENT CONFORMANCE

Subject	Description
Safety Standards	
CSA	Electrical Bulletin
FM	Electrical Utilization Standard Class 3820
ANSI C39.5	Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation
IEC 348 (2nd edition)	Safety Requirements for Electronic Measuring Apparatus
Regulatory Requirement	
VDE 0871 Class B	Regulations for RFI Suppression of High Frequency Apparatus and Installations

INSTALLATION, PREPARATION FOR USE, REPACKAGING AND STORAGE

INTRODUCTION

This section contains unpacking, installation, power requirements, repackaging information, and long- and short-term storage for the 494/494P Spectrum Analyzer.

UNPACKING AND INITIAL INSPECTION

Before unpacking the 494/494P from its shipping container or carton, inspect for signs of external damage. If the carton is damaged, notify the carrier. The shipping carton contains the basic instrument and its standard accessories. Refer to the Standard Accessories list in Section 1 of either the Operators or Service Vol. 1, manual. The list with illustrations is also in Volume 2 of the Service manual following the Mechanical Parts Replacement listing.

If the contents of the shipping container are incomplete, if there is mechanical damage or defect, or if the instrument does not meet operational check requirements, contact your local Tektronix Field Office or representative. If the shipping container is damaged, notify the carrier as well as Tektronix, Inc.

The instrument was inspected both mechanically and electrically before shipment. It should be free of mechanical damage and meet or exceed all electrical specifications. Procedures to check functional or operational performance are in the Operation section. Performing the functional check procedure verifies instrument is operating properly. This check should satisfy the requirements for most receiving or incoming inspections. A detailed electrical performance verification procedure in the Service instructions provides a check of all specified performance requirements, as listed in the Specification section.

The 494/494P can be installed in any position that allows air flow in the bottom and out the rear of the instrument. Feet on the four corners allow ample clearance even if the instrument is stacked with other instruments. A fan draws air in through the bottom and expels air out the back. Avoid locating the instrument where paper, plastic, or like material might block the air intake.

The front panel cover provides a dust-tight seal and convenient place to store accessories and external waveguide mixers. Use the cover to protect the front panel when storing or transporting the instrument. The cover is removed by first pulling up and in on the two release latches, then pull up on the cover. The door to the accessories compartment is unlatched and opened by pressing the latch to the side and lifting the cover.

The handle of the 494/494P can be positioned at several angles to serve as a tilt stand, or it can be positioned at the top rear of the instrument between the feet and the rear panel, so instruments can be stacked. To position the handle, press in at both pivot points and rotate the handle to the desired position.

CAUTION

Removing or replacing the cabinet on the instrument can be hazardous. The cabinet should only be removed by qualified service personnel. Removal instructions are contained in the Maintenance section.

Installation instructions for the rackmount/benchtop versions of the instrument are described in the Options Section of this manual. Refer installation to qualified service personnel.

CAUTION

If the rackmount version is extended out of the rack and tipped up to gain access to the bottom or back panels of the cabinet, it can fall back into the rack unless it is held. Use care when doing this to avoid damaging the front panel or equipment that may be mounted above the 494/494P.

POWER SOURCE AND POWER REQUIREMENTS

The 494/494P is designed to operate from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Operating from power sources where both current-carrying conductors are isolated or above ground potential (such as phase-to-phase on a multi-phase system or across the legs of a 110-220 V single-phase, three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit. Refer to the Safety Summary at the front of this manual.

The ac power connector is a three-wire polarized plug with the ground (earth) lead connected directly to the instrument frame to provide electrical shock protection. If the unit is connected to any other power source, the unit frame must be connected to an earth ground.

The 494/494P can be operated from either 115 Vac or 230 Vac nominal line voltage with a range ot 90 to 132 or 180 to 250 Vac, at 48 to 440 Hz. Power and voltage requirements are printed on a back-panel plate mounted below the power input jack.

WARNING

Only qualified service personnel should attempt to change the power input requirements. Unfamiliarity with safety procedures can result in personal injury. Refer to the Safety Summary at the front of this manual.

Input power requirements are changed with a switch on the back panel (see Figure 3-1) and the replacment of the input line fuse, F301. F301 is a 4A fast blow for 115 Vac nominal, and 2A slow blow for 220 Vac nominal.

Remove the protective cover and position the switch to the desired setting.

Remove the holder and line fuse and replace with a fuse that is rated according to the input voltage specification.

The power cord should also be replaced. Figure 3-2 illustrates these power cord options and the following table lists there part number.

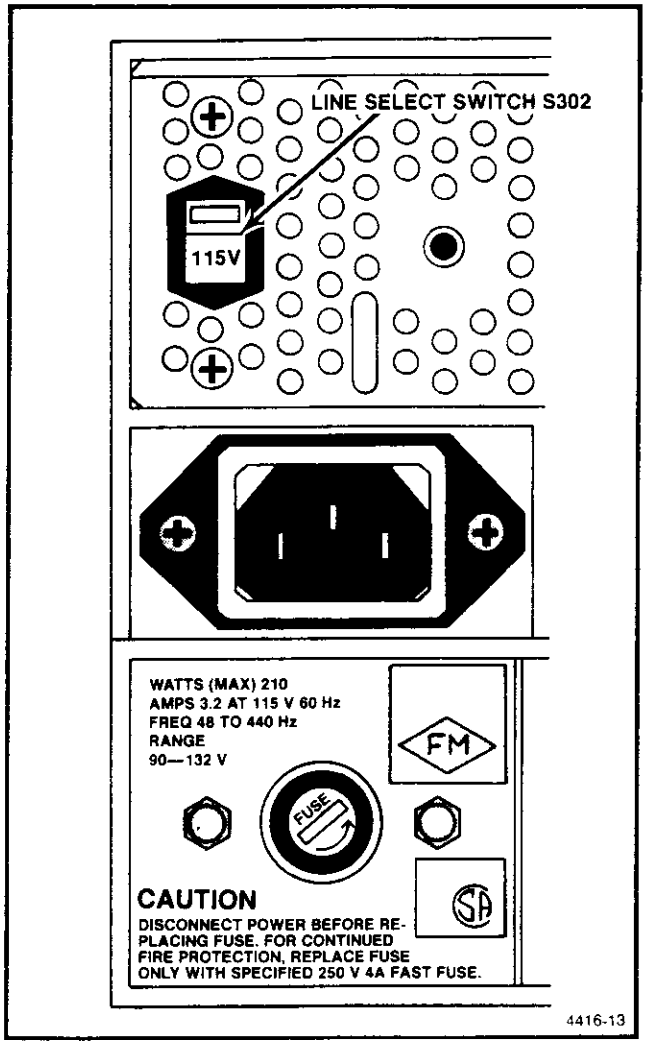


Figure 3-1. Location of input power selector switch and line fuse.

Power Cord Options

Option	Description	P/N
A1	Universal Euro, 220 V/50 Hz @ 16A	161-0132-00
A2	United Kingdom U.K., 240 V/50 Hz @ 13A	161-0133-00
A3	Australian, 240 V/50 Hz, @ 10A	161-0135-00
A4	North American, 240 V/60 Hz, @ 12A	161-0134-00
A5	Swiss, 250 V/50 Hz, @ 6A	161-0167-00

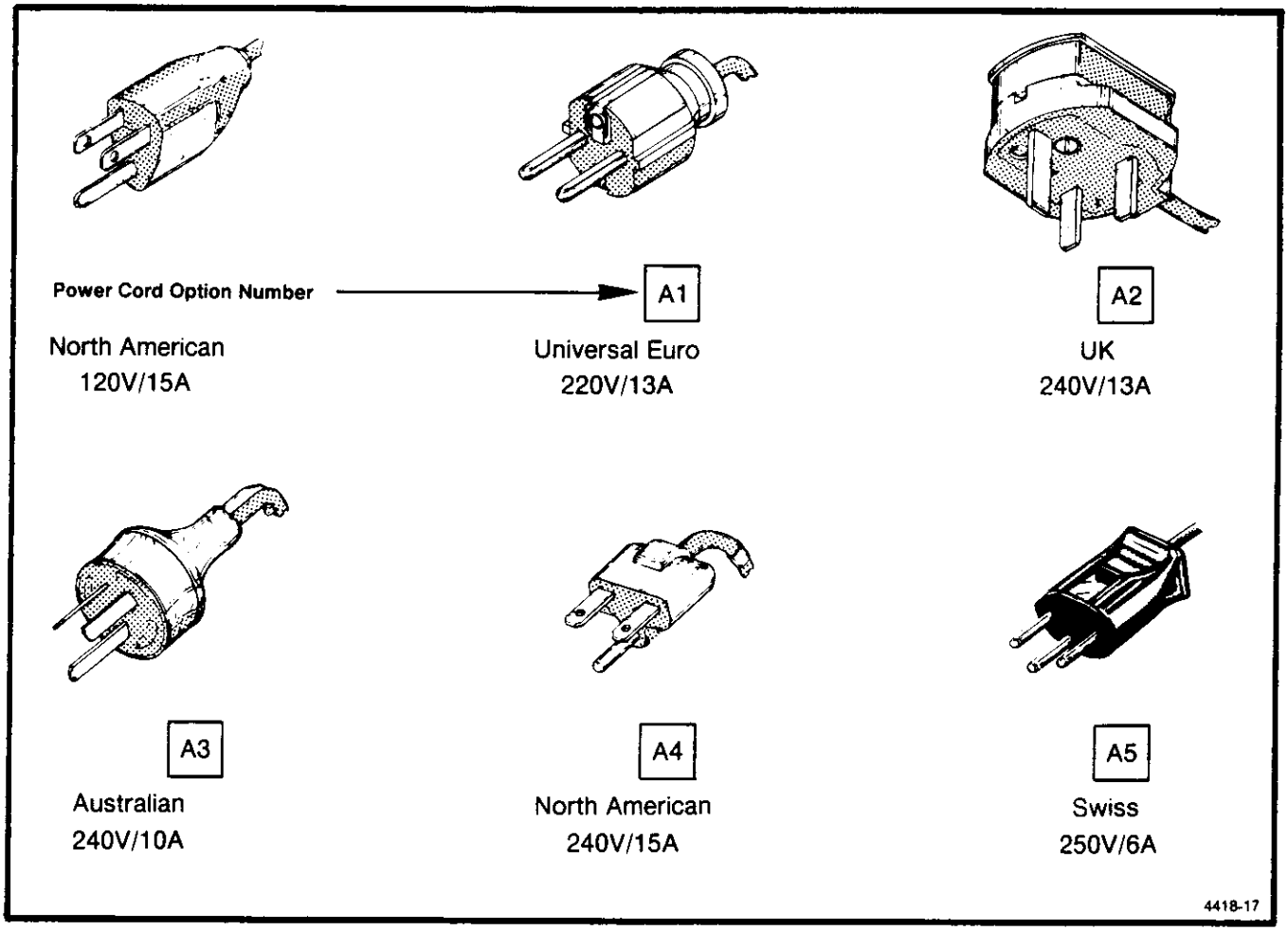


Figure 3-2. International power cord and plug configuration for the 494/494P.

REPACKAGING FOR SHIPMENT

When the 494/494P is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner and address, name of individual at your firm that can be contacted, complete serial number, and a description of the service required. If the original package is unfit for use or not available, repackage the equipment as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions that are at least six inches more than the equipment dimensions, to allow for cushioning. Table 3-1 lists instrument weights and the carton strength requirements.

2. Install the front cover and surround the instrument with polyethylene sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or urethane foam between the carton and the sides of the instrument.

4. Seal with shipping tape or industrial stapler.

Table 3-1
SHIPPING CARTON TEST STRENGTH

Gross Weight		Carton Test Strength	
Pounds	**Kilograms**	**Pounds**	**Kilograms**
0-10	0-3.73	200	74.6
10-30	3.73-11.19	275	102.5
30-120	11.19-44.76	375	140.0
120-140	44.76-52.22	500	186.5
140-160	52.22-59.68	600	223.8

If you have any questions, contact your local Tektronix Field Office or representative.

STORAGE

Short Term

There are no requirements for short term storage (less than 90 days) other than store the instrument in an environment that meets the non-operating environmental specifications.

Long Term

If you plan to store the instrument for more than 90 days, retain the shipping container to repackage the instrument. The battery in the instrument is lethium, which does not require removal. Package the instrument in a vapor bag with dessicant and store in a location that meets the environmental non-operating specifications.

PERFORMANCE CHECK

INTRODUCTION

The procedures in this section verify that the instrument is performing according to the characteristics that have limits and performance requirements as specified under the Performance Requirement column in the Specifications section. Some of the non-specified parameters and instrument functions are also checked. This check verifies that the instrument is calibrated and will perform as described. All tests can be performed without access to the interior of the instrument.

Checks should be performed in sequence because some tests rely on the satisfactory performance of related circuits, and the procedures are arranged to minimize test equipment setup. If a performance measurement is marginal or below specification, an adjustment procedure to optimize the circuit performance will be found, under a similar heading, in the Adjustment section. After adjustment, recheck the performance. We recommend adjusting only those circuits that do not meet performance criteria.

If adjustment fails to return the circuit to specified performance, refer to the Maintenance section for troubleshooting and repair procedures.

Procedures that are unique to instrument options, are described as a sub-part of the step within this section.

INCOMING INSPECTION TEST

The Operators manual contains an operational or functional check that checks all functions of the 494/494P. This check is recommended for incoming inspections because it requires no external equipment or special expertise and is a reliable indication that the instrument is performing properly.

VERIFICATION OF TOLERANCE VALUES

Compliance tests, of those limits listed in the Performance Requirement column of the instrument specifications, shall be performed after sufficient warm-up time and completion of preliminary preparation steps (such as front-panel adjustments). Measurements shall be performed by instruments that do not affect the values measured.

Measurement tolerance of test equipment should be negligible in comparison to the specified tolerance; and, when not negligible, the error of the measuring apparatus shall be added to the tolerance specified.

HISTORY INFORMATION

The instrument and manual are periodically evaluated and updated. If modifications require changes in the procedures, information applicable to earlier instruments will be included within a step or as a sub-part to a step.

EQUIPMENT REQUIRED

Table 4-1 lists the test equipment and calibration fixtures recommended for the Performance Check. This equipment is also applicable for the adjustment procedures in the next section. The characteristics specified are the minimum required for the checks. Substitute equipment must meet or exceed these characteristics. Special calibration fixtures are listed because they facilitate the procedure. These fixtures are available from Tektronix, Inc., and may be ordered through your local Tektronix Field Office or representative.

Because some characteristics may require sophisticated tests equipment and/or procedures to accurately measure which may not be practical. In this case a compromise may be made in these procedures to facilitate checking the characteristic. If this is the case a statement or footnote to this fact is added to the step. The more exact method of measuring the characteristic can be supplied by your Tektronix Service Center.

Table 4-1
EQUIPMENT REQUIRED

Equipment or Test Fixture	Characteristics	Recommendation and Use
	PERFORMANCE CHECK	
Test Oscilloscope	Vertical sensitivity, 50 mV/Div to 5 V/Div	Any TEKTRONIX 7000-Series oscilloscope with plug-in units for real-time display such as: 7A11/7B50A, and P6108 1X Probe (used to monitor signal and voltage levels)
Two (2) Time Mark Generators	Marker output, 1 s to 1 μs; accuracy 0.001%	TEKTRONIX TG 501 with TM 500-Series Power Module (used to check time/div and span accuracy)
Digital Counter	0 to 200 MHz, 1 Hz resolution, 25 mV sensitity. Must have an internal or external reference oscillator with an absolute accuracy that is better than 10^{-9}	TEKTRONIX DC 510 or 5010 with TM 504 Power Module, or Hewlett-Packard 5316A (used to measure Calibrator frequency)
Function or Sine-Wave Generator	1 Hz to 1 MHz; 0 to 20 V - p-p	TEKTRONIX FG 503 Function Generator (used to check external trigger and horizontal input requirements)
Signal Generator(s)	10 Hz to 10 MHz,constant output. 250 kHz-110 MHz, leveled output Two (2) 500 kHz to 2.0 GHz generators calibrated and leveled. Output, −100 dBm to +10 dBm; spectral purity 60 dB or more below the fundamental.	Hewlett-Packard Model 654A (used to check attenuator and gain accuracy) TEKTRONIX SG 504, Hewlett-Packard Model 8640A/B and Model 8614A generators (used to check frequency response; and as a signal source for IM and display accuracy checks)
Sweep Oscillator	.01 to 21 GHz; frequency response, ±1.0 dB, or 2.0 to 21 GHz (with 500 kHz to 2.0 GHz generators)	Hewlett-Packard Model 8350A with Model 83595A Option 002 Plug-in; or. 8620C and 86290B Option 40 Plug-in (used to check frequency response and flatness)
Power Divider	Dc to 22 GHz	Wienchel Model 1579B
Coaxial Detector	.01 to 26 GHz	Hewlett-Packard Model 8473C
Power Meter with Power Sensors	−60 dBm to −20 dBm full scale; 100 kHz to 26 GHz	Hewlett-Packard Model 435A or 436A with 8482A and 8485A Power Sensors
Vector Voltmeter or Power Meter with Low-pass Filter	Frequency to 100 MHz Measure −20 dBm, within ±0.1 dB. The filter must have rolloff of 40 dB or more at 200 MHz.	Hewlett-Packard Model 8405A (used to check CALibrator OUTput) Hewlett-Packard Model 435A with 8482A Sensor (used to check CALibrator Output). Filter: Texscan or Lark

Table 4-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
	PERFORMANCE CHECK (cont)	
UHF Comb Generator	Provide comb line to 18 MHz; accuracy 0.0%	TEKTRONIX Calibration Fixture 067-0885-00 with TM 500 Power Module (used to check frequency readout accuracy)
Spectrum Analyzer	Frequency range, 50 kHz - 2.2 GHz	TEKTRONIX 492, 494.or 7L18, 7L14 Option 39 (used to check compression point)
One 10 dB and One 1 dB Step Attenuator	Range, 0-110 dB, in 10 dB and 1 dB steps; accuracy ±0.1 dB; frequency range, dc - 18 GHz	Step attenuator; such as Hewlett Packard 8494B and 8496B with 11716A inter connect kit, calibrated by precision standard attenuators; such as Weinchel Model AS-6 attenuator (used to check RF attenuator)
Step Attenuator One (1)	Range, 0 - 12 dB, in 1 dB steps; dc - 1 GHz, accuracy ±0.25 dB to 0.5 GHz	Hewlett Packard 355C (used to check input compression)
Attenuator (SMA connectors)	3 dB, 50 Ω; dc to 20 GHz	Weinchel Model 4M. Tektronix connectors) Part No. 015-1053-00
Two attenuators (bnc connectors)	20 dB, 50 Ω; dc to 2.0 GHz	Tektronix Part No. 011-0059-02
Coaxial cable (50 Ω. 5 ns, sma connectors)		Tektronix Part No. 015-1006-00
Adapter (N male to sma male)		Tektronix Part 015-0369-00
Adapter (N male to No. bnc female)		Tektronix Part 103-0045-00
"T" Connector (bnc)		Tektronix Part No. 103-0030-00
Coaxial Cables (50 Ω) two required		Tektronix Part No. 012-0482-00
	ADJUSTMENTS	
All the items listed above plus the following are required for the Adjustment Procedure.		
Return Loss Bridge	10 MHz to 1 GHz, 50 Ω	Wiltron VSWR Bridge Model 62BF50
Microwave Frequency Counter	10 Hz to 10 GHz, −20 dBm sensitivity	Hewlett-Packard Microwave Counter Frequency Counter 5342A (used to measure the 2nd LO frequency)
Attenuator (3 dB miniature)	Frequency to 5 GHz; connectors 5 mm	Weinchel Model 4M, Tektronix Part No. 015-1053-00

Table 4-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
	ADJUSTMENTS (cont)	
Autotransformer	Capable of varying line voltage from 90 to 130 V_{ac}	General Radio Variac Type W10MT3
Digital Multimeter Dc Block	10 μV to 350 V dc	TEKTRONIX DM 501A or DM 502A. Tektronix Part No. 015-0221-00
Adapter (Sealectro male to male)		Tektronix Part 103-0098-00; Sealectro Part No.51-072-0000
Adapter (bnc female to Sealectro male)		Tektronix Part No. 103-0180-00
Three Extension Cables (Sealectro female to Sealectro male)		Tektronix Part No. 175-2902-00
Adapter (bnc to No. Sealectro)		Tektronix Part No. 175-2412-00
Adapter (bnc female to sma male)		Tektronix Part No. 015-1018-00
Cable (20″), Tip plugs to bnc		Tektronix Part No. 175-1178-00
Coaxial cable (8″)		Tektronix Part No. 012-0208-00
Screwdriver, tuning		Tektronix Part No. 003-0675-00
Alignment tool		Tektronix Part No. 003-0968-00 (square-pin adjustment tool for VR calibration
Screwdriver, flat, 6″ with 1/8″ tip		
Screwdriver, Phillips No. 1		
Allen wrenches (3), 3/32″, 5/64″, 7/64″		
Service Kit (Extender boards)[a]		Tektronix Part No. 672-0865-00.

[a] **These fixtures are part of the Service Kit 006-3286-00 listed in the Maintenance section.**

PRELIMINARY PREPARATION

1. Firmware Version

During initial turn-on or power-up cycle, the instrument and the front panel processor firmware versions are displayed on the crt for approximately two seconds. The Replacement Parts List in the Service manual, Volume 2, lists the ROMs used for each version. The service manual also lists the firmware operating notes associated with each firmware version.

2. Error Message Readout

If the microcomputer detects a hardware failure, a failure report will come on screen and remain for about 2 seconds. A status message will then appear and remain for the duration of the failure. Press HELP to obtain an error message that explains the impact of the failure on instrument operation. If the processor cannot set the oscillator frequency, due to a hardware failure, it will continue to try each sweep. The sweep holdoff time will increase substantially as it trys. To disable attempted oscillator corrections, press <SHIFT> and then FREE RUN. Center frequency accuracy specifications will not be met in this mode. Pressing <SHIFT> FREE RUN again will re-enable oscillator correction routines. Another failure message will appear if the failure has not been corrected. The following are other error messages that may appear:

CALIBRATION FAILED — see Reference Level and Frequency Calibration part of the CAL routine.

COUNTER FAILURE — either a hardware problem will not allow the counter to work or there is insufficient signal level for a count.

POWER SUPPLY FAILURE — one or more of the power supplies is out of regulation.

NON-VOLATILE RAM CHECK SUM ERROR — a checksum error on data in this memory has occurred. Either the CMOS RAM has not been initialized with data for the first time or the battery or the RAM has failed.

3. Initial Turn-on

a. Connect the 494/494P power cord to an appropriate power source (see "Power Requirements" under Installation and Repackaging, in Section 3) and switch POWER on.

b. When POWER is switched on (power up), the processor will run a memory and I/O test. If a problem exists, a failure message will appear on screen. By pressing the continue key, as directed in the message, the operator can bypass the failed test and attempt to use the instrument; however, performance may not be as specified. The program will complete in about 6 seconds and the instrument will be ready to operate if there is not a problem. Note that the crt readout is functioning.

4. Calibrate Center Frequency, Reference Level, and Dynamic Range

NOTE

When the <SHIFT> CAL function is activated, the 494/494P microcomputer performs a center frequency and reference level calibration. This calibration is required before the instrument will meet its center frequency and reference level accuracy performance specifications. A recalibration should be done any time the ambient temperature changes from the last calibration and at regular intervals to ensure that the instrument frequency and amplitude measurements are accurate. An explanation of Reference Level Accuracy, with respect to ambient temperature, is described in the Specifications section.

After the microcomputer has completed a calibration routine, the results can be observed by pressing <SHIFT> MIN NOISE. The "Internal Calibration Result" message shows the correction factor used to center the resolution bandwidth filters and to bring the amplitude level within 0.4 dB of the 1 MHz filter.

a. Press the <SHIFT> CAL to start the calibration routine. A message on the crt will direct the user how to adjust the Vertical and Horizontal POSITION, AMPL and LOG CAL potentiometers. This sets the absolute Reference Level for the 1 MHz resolution bandwidth filter. An automatic calibration is then run by the microcomputer, which measures and corrects frequency and amplitude errors of the other filters with respect to the 1 MHz filter and the reference frequency. As stated above, these correction factors are held in non-volatile memory. Press FINE to continue or <SHIFT> to exit the routine.

b. If the processor can complete the routine, the instrument control settings will return for normal operation. If a CALIBRATION FAILED message appears, refer to the correction factors by pressing <SHIFT> MIN NOISE.

If any amplitude correction factor, at room temperature, for a filter is greater than 1 dB, the filter in the VR assembly should be readjusted. Refer to the Adjustment Procedure section.

PERFORMANCE CHECK PROCEEDURE

1. Check Operation of Front Panel Pushbuttons and Controls

Shift Functions — In the shift mode, those buttons with two or more functions, indicated by the blue and/or orange lettered nomenclature beside the button, activate the shift function when pressed. In some cases a parameter or command is entered followed by data, via the Data Entry keyboard, then terminated with a multiplier, unit value, or display scale factor.

The following procedures check the operation of all front panel pushbuttons, selectors, and controls. The buttons should illuminate when the function is active.

a. Set the FREQUENCY to 100 MHz, REF LEVEL to −20 dBm, and FREQ SPAN/DIV to 20 kHz. Apply the CAL OUT signal to the RF INPUT, by using the 50 Ω cable and bnc-to-N adapter, then change the Vertical Display to 2 dB/DIV.

b. Note that the following pushbuttons and controls operate as described when they are activated.

INTENSITY — Rotate the control through its range and note crt beam brightness change.

READOUT — When this button is not illuminated, off mode, crt readout is off. In the active state (button illumintated), there is crt readout of REF LEVEL, FREQUENCY, FREQ SPAN/DIV, VERT DISPLAY, RF ATTEN, FREQ RANGE, REFERENCE OSCILLATOR, and RESOLUTION BANDWIDTH. The INTENSITY control changes the brightness of readout characters as well as the display.

GRAT ILLUM — When activated (active state) the graticule is illuminated. In the off mode the graticule lights are dim.

BASELINE CLIP — When activated (illuminated) the baseline of the display, up to about one graticule division, is clipped (blanked).

Triggering — Triggering mode is activated by pressing one of four pushbuttons. Button illuminates when in the active state. Pressing any one of the buttons cancels or deactivates the other mode.

FREE RUN — Trace free runs.

INT — Sweep is triggered when noise level or modulation amplitude of a signal is ≥2.0 division. Triggering is checked near the end of this procedure.

LINE — Trace is triggered at power line frequency. Switch Triggering mode to LINE and note sweep is triggered.

EXT — The trace runs only when an external signal, ≥1.0 V peak, is applied to the back panel External HORIZ/TRIG connector. Since external test equipment is required to check this function, a check is not included at this time.

SINGLE SWEEP — When activated, single sweep aborts the current sweep; pressing the button again will arm the sweep generator and light the READY indicator. The indicator will remain lit until the sweep has run. When triggering conditions are met, after the circuit is armed, the analyzer will make only one sweep. Single sweep mode is canceled when any Triggering button is pressed. The effect of SINGLE SWEEP may be more apparent with digital storage.

a. Press FREE RUN Triggering and set the TIME/DI 0.5 s.

b. Press SINGLE SWEEP and note that the sweep aborts.

c. Press SINGLE SWEEP again and note that the READY indicator lights and the sweep runs.

d. Press FREE RUN to cancel single sweep and return the TIME/DIV to AUTO position.

TIME/DIV — This control selects sweep rate, manual scan, and external sweep operation. In the MNL position, MANUAL SCAN control should move the crt beam across the full frequency span or horizontal axis of the crt graticule. In the EXT position a voltage of 0 to +10 V, applied to the rear panel HORIZ/TRIG connector, should deflect the crt beam across the full 10 division screen.

Vertical Display — Display modes are activated by three pushbuttons. Pressing any of these buttons cancels the other mode.

10 dB/DIV — When this button is activated, the display is a calibrated 10 dB/division with an 80 dB dynamic range.

(a) With a REF LEVEL of −20 dBm, activate 10 dB/DIV and AUTO RESOLN. Set the FREQ SPAN/DIV to 20 kHz and tune the calibrator signal to center screen.

(b) Change REF LEVEL and note that the display steps in one division increments, representing 10 dB/division. Return the REF LEVEL to −20 dBm.

2 dB/DIV — When this button is pressed, the display is a calibrated 2 dB/division with 16 dB of dynamic range.

(a) Activate the 2 dB/DIV mode and change the REF LEVEL to −6 dBm.

(b) Note that the display steps 1.0 division for each two steps of the REFERENCE LEVEL control.

(c) Return the REF LEVEL to −20 dBm.

LIN — When this button is actived, the display is linear between the reference level (top of graticule) and zero volt (bottom of graticule); the crt VERT DISPLAY reads out in volts/division.

Activate the LIN mode and note that the Vertical Display readout changes to 2.80 mV/division.

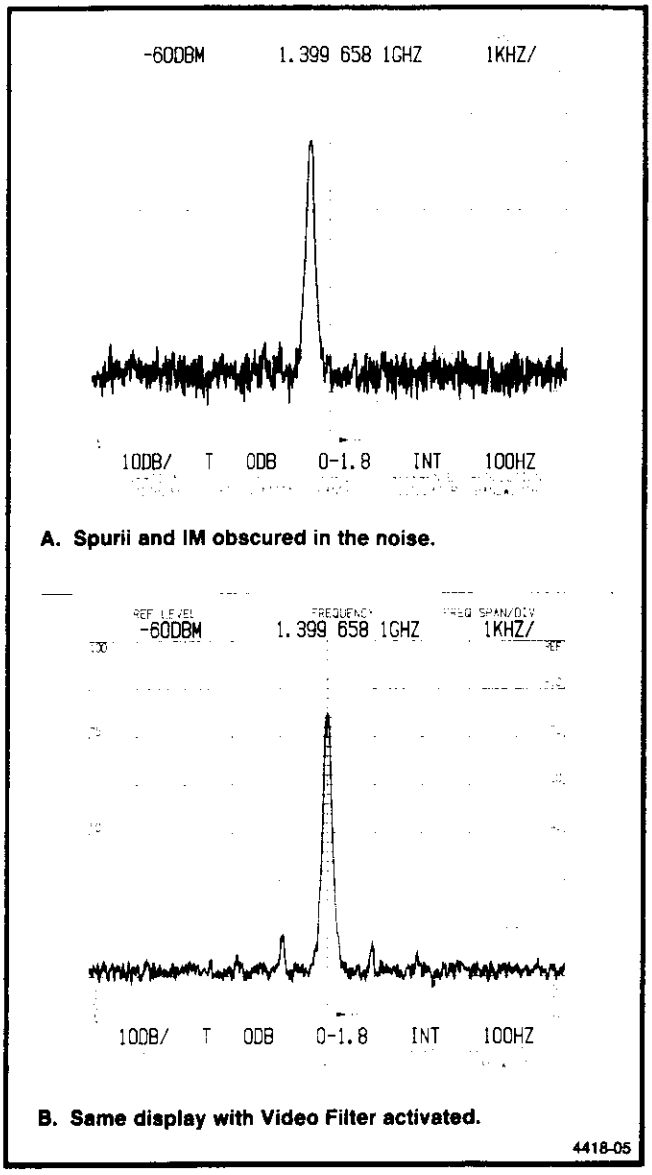
PULSE STRETCHER — When activated, the fall-time of video signals increases so narrow video pulses will show on the display. This function is checked later with external test equipment.

Video Filter — Two filters can be independently selected to provide, WIDE or NARROW (1/30th or 1/300th of the resolution bandwidth) filtering to average the noise.

(1) Change the FREQ SPAN/DIV to 500 kHz, activate 10 dB/DIV and AUTO RESOLN, and tune the calibrator signal to center screen.

(2) Activate WIDE and NARROW Video Filters and note the reduction in noise as each filter is switched in (see Figure 4-1). The NARROW filter will have a more pronounced effect on noise reduction. Also note the change in sweep rate, if the TIME/DIV selector is in the AUTO position.

(3) Switch both Video Filters off.



A. Spurii and IM obscured in the noise.

B. Same display with Video Filter activated.

Figure 4-1. Video Filter effect on VSWR.

DIGITAL STORAGE — Either one or both the "A" and "B" waveforms, from digital storage, can be selected. The amplitude of a signal should remain constant when digital storage is switched on (VIEW A or VIEW B activated). The PEAK/AVERAGE control positions a cursor over the vertical window of the screen Noise and signal level will be averaged below the cursor and peaked above the cursor. Check operation according to the following description.

VIEW A — When pressed, the "A" waveform, from digital storage, is displayed. With SAVE A off, the "A" waveform is updated each sweep as the beam travels from left to right. With SAVE A on, the waveform and readout are not updated.

VIEW B — When actived, the "B" waveform is displayed. When both VIEW A and VIEW B are active, the "A" and "B" waveform are interlaced and displayed. Both waveforms are updated each sweep. Update of the "A" waveform depends on the state of SAVE A.

SAVE A — When actived, the "A" waveform, with its readout, is saved. In this mode the data for "A" waveform is not updated each sweep. Switch VIEW B off then change REF LEVEL and note that the "A" display does not change. The readout for the saved waveform will be displayed anytime SAVE A is on and VIEW B and B−SAVE A are off. If either VIEW B or B—SAVE A is on, the readout reflects current analyzer setup.

MAX HOLD — When on, the maximum signal amplitude at each memory location is stored. The waveform is updated only when signal data is greater than that previously stored. Verify operation by changing FREQUENCY or REF LEVEL and note that the maximum level at each location is retained.

B−SAVE A — The arithmetic difference between an updated "B" waveform and a SAVE A waveform is displayed. SAVE A function is also activated when B−SAVE A is pressed.

Press B−SAVE A then change the REF LEVEL so the difference between the "B" and SAVE A waveform is displayed with VIEW A and VIEW B off. The reference (zero difference) level is factory set at graticule center. The position of this reference level can be changed by qualified service personnel. Positive differences between the two displays appear above and negative differences below the line.

PEAK/AVERAGE — When digital storage is on, this control positions a horizontal line or cursor over the vertical graticule window. Signals above the cursor are peak detected, signals below the cursor are averaged by the digital storage. Verify operation by moving the cursor within the noise level and note the noise amplitude change as the cursor is positioned.

IDENTify — When the identify function is activated, every other sweep, with its waveform, is vertically displaced from the other. The frequencies of the 1st and 2nd local oscillators are moved such that true signals are not displaced horizontally on alternate sweeps while spurious signals are shifted 100 MHz or more, which is off screen for the narrower spans. The FREQ SPAN/DIV must be 50 kHz or less for the coaxial bands and 50 MHz or less for the waveguide bands (21 GHz or more) before the processor will activate the Identify mode.

(1) With the 500 MHz marker tuned to center frequency, decrease the FREQ SPAN/DIV to 50 kHz or less and press IDENT.

(2) Note that there is no horizontal displacement of the 500 MHz signal on alternate sweeps. To help determine if the signal is true or false,decrease the sweep rate or activate SAVE A, with both VIEW A and VIEW B on, so a comparison is easily observed (see Figure4-2).

(3) Switch IDENT off.

AUTO RESOLN — When this function is on, resolution bandwidth automatically changes to maintain a calibrated display, as FREQ SPAN/DIV and TIME/DIV are changed. Check operation by changing FREQ SPAN/IV or TIME/DIV settings and note the RESOLUTION BANDWIDTH change. UNCAL indicator should not light over the FREQ SPAN/IV range if the TIME/DIV selector is in AUTO position.

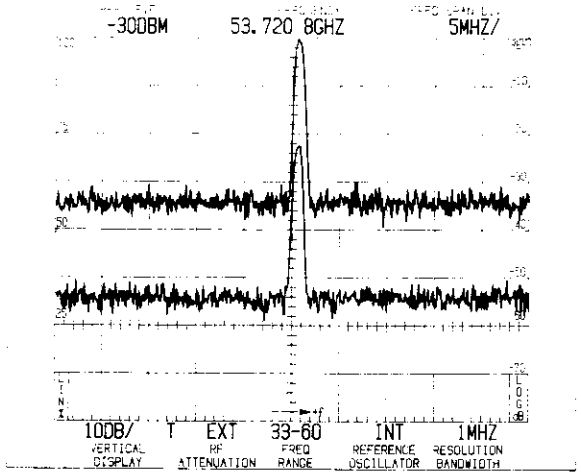
MAX SPAN — When this function is activated, the span switches to maximum and the analyzer sweeps the full band. When deactivated, the span/div will return to its previous setting.

ZERO SPAN — When this button is activated, the span should shift to zero for a time-domain display. When deactivated, the span returns to its previous setting.

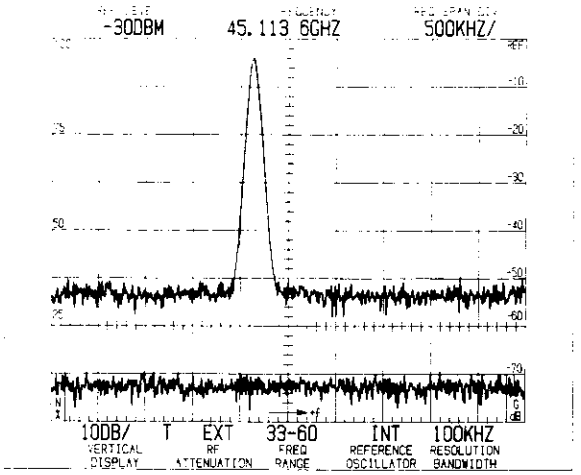
FREQUENCY SPAN/DIV — As this control is rotated, the Span/Div should change from Max to 0, counter clockwise from MAX position, in a 2, 1, 5 sequency. The display should indicate this change.

RESOLUTION BANDWIDTH — As this control is rotated from the 30 Hz position, the resolution bandwidth should change from 30 Hz to 100 Hz and then in decade steps to 1 MHz.

REFERENCE LEVEL — In the 10 dB/DIV Vertical Display mode, with FINE off, the REF LEVEL should step in 10 dB increments as the control is rotated. When FINE is activated, the steps are 1 dB. In the 2 dB/DIV mode, the



A. Typical response of a true or real signal.



B. Typical response from a false signal. Signal for bottom sweep is off screen.

4418-06

Figure 4-2. Typical display with SAVE A on to observe IDENTify mode.

steps are 1 dB, with FINE off, and 0.25 dB with FINE active. When the Vertical Display factor is 4 dB/div or less, with FINE on, the analyzer should switch to the delta A mode where the REF LEVEL readout goes to 0.00 dB then steps in 0.25 dB increments as the REFERENCE LEVEL control is rotated in a clockwise direction. Note, the REF LEVEL dB reading does not go above 0.00 dB if the control is rotated counterclockwise.

(1) Set the MIN RF ATTEN to 0 dB, Vertical Display to 10 dB/DIV, and rotate the REFERENCE LEVEL control counterclockwise to +30 dBm then clockwise to −110 dBm.

(2) Note that the REF LEVEL readout changes in 10 dB increments.

(3) Press FINE and rotate the REFERENCE LEVEL counterclockwise to −117 dBm. Note the REF LEVEL now steps in 1 dB increments.

(4) Press <SHIFT> REF LEVEL and select −30 dBm with the Data Entry keyboard, then press <SHIFT> dB/DIV and enter 4 dB, with the Data Entry keyboard. Press FINE and note that the REF LEVEL goes to 0.00 dB.

(5) Rotate the REFERENCE LEVEL control clockwise and note the REF LEVEL now steps in 0.25 dB increments from the 0.00 dB reference.

(6) Continue turning the control until the REF LEVEL reads −10 dBm then press 10 dB/DIV and deactivate FINE.

(7) Return the REF LEVEL to −20 dBm and note that 10 dB of RF ATTEN is switched in at a REF LEVEL of −20 dBm. This prevents signal compression of any signals whose amplitude is within the graticule area.

MIN RF ATTEN — This control sets the minimum amount of RF attenuation in the signal path, regardless of the REF LEVEL setting. Verify proper operation by setting the MIN RF ATTEN dB selector to 20 and change the REF LEVEL settings. Note that the RF ATTEN readout does not go below 20 dB.

FINE — When this button is activated, the REFERENCE LEVEL steps decrease to the Fine mode as described and checked under Reference Level.

MIN NOISE/MIN DISTORTION — This button selects one of two algorithms that select attenuator and IF gain. MIN NOISE (button illuminated) reduces the noise level by reducing the RF attenuation 10 dB and decreasing IF gain 10 dB. MIN DISTORTION reduces IM distortion due to input mixer overload. The normal mode of operation is with minimum distortion. To observe any change, the amount of RF ATTEN, displayed by the crt readout, must be 10 dB higher than the MIN RF ATTEN selector setting.

(1) Set the REF LEVEL to −20 dBm and the MIN RF ATTEN at 0 dB. Note that the RF ATTEN readout indicates 10 dB.

(2) Activate MIN NOISE and note that the noise floor drops approximately 10 dB and the RF ATTEN readout changes to 0 dB. Deactivate MIN NOISE mode.

UNCAL — This indicator lights when the display is uncalibrated.

(1) Set the TIME/DIV to 50 ms, deactivate the AUTO RESOLUTION, and set the RESOLUTION BANDWIDTH to 10 kHz.

(2) UNCAL indicator should light and remain lit until the FREQ SPAN/DIV is reduced to 200 kHz or the RESOLUTION BANDWIDTH is increased to 1 MHz.

(3) Return the TIME/DIV to AUTO, press AUTO RESOLN, and set the FREQ SPAN/DIV to 100 MHz.

SHIFT — Pressing this button shifts those pushbuttons with more than one function, to their secondary function. The function of this secondary mode is nomenclated in blue or orange lettering next to the pushbutton. The shift mode deactivates after the function has been performed. SHIFT is also used to abort from menus or other multi-key functions.

HELP — When activated, pressing or operating any control or selector produces a help message on the crt that explains the function. Help messages will also prompt the user to the next operational move or explain any error message that may appear. Activate this mode and press various buttons to observe the applicable crt messages. Press the button again to cancel. <SHIFT> HELP lists current errors.

RECALL SETTINGS/STORE — When pressed in the "Recall Settings" mode, this button will produce a listing of the memory registers and the center frequency of the setup stored. The 0 register retains the power-down settings. All can be recalled after power-up. In the <SHIFT> STORE mode, the existing front panel setup is stored in one of nine selected locations. A listing of all registers with the center frequency of the stored setup is displayed. A blank entry indicates no settings stored.

(1) Press <SHIFT> STORE, then select register number 1 to store the current front panel setup.

(2) Change front panel control and selector settings.

(3) Press RECALL and select the Data Entry key 1, to recall the setup.

(4) Note that the instrument front panel set-up returns to that previously entered.

COUNT/COUNT RESOLN — A count for any signal below the dot marker, that is 20 dB above the noise floor and no more than 60 dB down from the REF LEVEL, is made between each sweep with the counter on (button illuminated).The counted signal frequency appears in place of the center frequency. <SHIFT> COUNT RESOLN allows the selection of the counter resolution to 1 Hz, via the Data Entry keyboard.

(1) Set the FREQUENCY to 100 MHz. Establish a counter resolution of 100 Hz by pressing <SHIFT> COUNT RESOLN and enter 100 Hz, via the Data Entry keyboard.

(2) Tune to any signal that is 20 dB or more above the noise level and less than 60 dB down from the REF LEVEL. Activate COUNTER and note that the frequency readout has a resolution of 100 Hz.

ΔF — When the Δ F function is activated, center FREQUENCY readout initializes to 0.0 MHz or 0.00 kHz depending on the FREQ SPAN/DIV setting. The frequency difference to another point in the span can now be determined by tuning that point to center screen and noting the readout. Check, by measuring the difference between calibrator markers. If the frequency is tuned below "0.0" the readout will indicate (−) sign. Deactivate and note that the readout returns to the previous center FREQUENCY.

COUNT→CF — This button is used when a close-in analysis of a signal, in narrow spans, is desired. When this pushbutton is pressed, the signal under the frequency dot is counted once (even if the COUNTER mode is inactive) then the Center Frequency is shifted to the counted frequency. Any Freq Span/Div can now be selected and the signal will remain centered on screen. The count resolution and the resulting accuracy of the tuning is equal to the current counter resolution.

(1) Decrease the FREQ SPAN/DIV and increase the RESOLUTION BANDWIDTH so the calibrator signal spans 3 or 4 divisions on the screen. Tune the signal so approximately 20 dB of signal level, above the noise floor, is under the dot.

(2) Press COUNT→CF and note that the signal moves under the frequency dot and the FREQUENCY readout changes to indicated the frequency of the marker.

FREQUENCY RANGE — These pushbuttons shift the 494/494P frequency range up or down from the current band. Press first one and then the other and note that the frequency bands change accordingly. If the operator selects FREQUENCY via the Data Entry keyboard, the microprocessor will automatically select the appropriate frequency range.

AUTO PEAK/EXT MIXER — Selects Auto Peaking in its primary mode, and External Mixer in the shift mode. When AUTO PEAK is activated (button illuminated) one of two things occur:

(1) If the analyzer is operating in the preselector bands (1.7 - 21 GHz), the preselector initiates a peaking routine on any signal within the center two divisions of

the screen. The algorithm peaks the preselector tuning for this center frequency setting, then stores this setting in non-volatile (battery powered) memory. If a signal is not on screen, the algorithm will revert to the code that was previously stored in memory; or, if there is no setting, to the mid point of the peaking range. After a center frequency setting for a band has been stored, the operator can then switch back to this band with the assurance that the preselector is peaked well enough to track the oscillator and provide reasonable sensitivity.

(2) If the analyzer is operating in the External Mixer mode, the peaking routine sets the external mixer bias so the response is peaked. If a signal is not present, the algorithm reverts to the previous bias setting stored in memory or, if there is no previous setting, it sets the bias voltage mid range.

When <SHIFT> EXT MIXER is pressed, External Mixer operation is initiated, which dc couples the EXTERNAL MIXER port to an internal bias source for external mixers, and ac couples the IF return from the external mixer to the 2nd converter. This bias voltage is either manually set, with the MANUAL PEAK control, or automatically set by the Auto Peak algorithm. When in the External Mixer mode, the crt readout for RF ATTEN reads EXT. To exit this mode, press <SHIFT> EXT MIXER. The REF LEVEL will shift to +30 dBm and the RF ATTEN to 60 dB to protect the internal mixer from high level signals that might be applied to the RF INPUT.

a. Auto Peak

(1) With the Calibrator signal applied to the RF INPUT, select a frequency of 3.0 GHz, by pressing <SHIFT> FREQ then 3 GHz, via the Data Entry keyboard. Select a REF LEVEL of −40 dBm, a FREQ SPAN/DIV of 10 kHz, and a RESOLUTION BANDWIDTH of 1 kHz.

(2) Peak the 3.0 GHz signal with the MANUAL PEAK control.

(3) Press AUTO PEAK. Note the message "PEAKING" on screen and the READY indicator for SINGLE SWEEP mode flash as the processor runs the auto peak routine.

(4) When complete, the signal amplitude should equal or exceed that obtained with manual peaking.

(5) Change bands by increasing or decreasing the FREQUENCY RANGE, then return to band 2. Note that auto peak maintains the setting stored in memory.

b. External Mixer

(1) Press <SHIFT> EXT MIXER, the analyzer should shift to the External Mixer mode (indicated by a readout of EXT above RF ATTEN). If AUTO PEAK mode is still active the button will remain lit as it does not indicate external mixer but auto peak status.

(2) Connect a voltmeter between the EXTERNAL MIXER port and ground. Measure the bias voltage. If in the Auto Peak mode, the bias should be a steady dc voltage. (If Auto Peak has not been run for this band, the bias voltage will read approximately −0.8 V or mid range.)

(3) Switch to the manual peak mode by pressing AUTO PEAK again. The button should not be illuminated and the bias voltage at the EXTERNAL MIXER port should now vary between approximately −2.5 V to +1.0 V, as the MANUAL PEAK control is rotated through its range.

(4) Press <SHIFT> EXT MIXER to deactivate EXTERNAL MIXER mode.

Setting Parameters via the Data Entry Keyboard

(1) Set the FREQ SPAN/DIV to 50 kHz and switch AUTO RESOLN on. Set the center frequency to 2.0 GHz by pressing <SHIFT> FREQ, then enter 2 GHz via the Data Entry keyboard. Note that the FREQUENCY sets to 2.000 GHz. (The number of digits is a function of the span/div or the count resolution if the counter is on.

(2) Enter frequencies of 200 MHz, 200 kHz, and 200 Hz by repeating the above procedure. Note that the FREQUENCY sets to that entered via the Data Entry keyboard.

(3) Set the SPAN/DIV to some setting via the keyboard and note that the entered Span/Div is set.

(4) Enter a REF LEVEL with the keyboard and note that the entry is set.

(5) Enter a desired Vertical Display factor with the keyboard and note that the keyed-in dB/div is set.

STORE DISPLAY and RECALL

Pressing <SHIFT> STORE DISP starts a sequence to store, either the "A" or "B" waveform and its associated readout, in a numbered (0-8) memory register. This informa-

tion is retained in non-volatile memory so it can be recalled at a later time. Informative messages, displayed on the crt, aid the user in completing the multiple button sequence. First a list of the center frequencies of current stored displays is shown. The number of digits in the readout is an indication of the Span/Div of each stored display (a greater resolution indicates a narrower span). A register without an associated frequency is empty. This display includes a prompt for the register number into which the display will be stored. The registser is selected, via the Data Entry keyboard, then a prompt asks which display ("A" or "B") to store in the selected register? Selection of the waveform completes the sequence and returns the instrument to normal operation.

To exit Store Display function press the <SHIFT> button. Pressing <SHIFT> RECALL recalls a selected waveform, with its readout, from memory, so it can be sent to the "A" or "B" part of digital storage. To see the display, activate the respective part of digital storage (VIEW A or VIEW B). The readout for the "A" waveform will only be shown if VIEW B and B−SAVE A are off, whereas the readout for a recalled "B" waveform will only be displayed if VIEW B or B−SAVE A are on. When RECALL is actived, SAVE A is also activated to protect the recalled waveform from overwrite if it is placed in "A" and to protect the current waveform if it is placed in "B". SINGLE SWEEP must be activated before a waveform is placed in "B", to prevent an overwrite by the next sweep. VIEW B must be activated to observe the recalled waveform in "B".

(1) Establish a display on the screen. Press <SHIFT> STORE DISPLAY then enter the memory register number (0-8) for the display and select display "A".

(2) Change the current display with the REF LEVEL or FREQUENCY control.

(3) Press <SHIFT> RECALL then select the register number that contains the above display (note the center frequency listing of the stored displays in each register). Press VIEW A and deactivate VIEW B.

(4) The recalled display, with its readout, should now become the "A" display. SAVE A should activate to save the display so the next sweep will not overwrite the recalled display. If VIEW B is on, both the recalled display (VIEW A) and the "B" display will be on screen. Since the most current display is the "B" waveform, the readout will depict the parameters for the "B" display. Switch VIEW B off so the readout will represent the recalled display.

(5) Activate SINGLE SWEEP then repeat part (3) except select "B" for the display. Activate VIEW B to view the recalled waveform.

(6) Repeat part (5) without activating SINGLE SWEEP and note that a message on screen warns that unless SINGLE SWEEP is on, the recalled display will be overwritten by the next sweep.

<SHIFT> PLOT (494P only)

When the 494P is connected to a plotter over the GPIB cable, pressing <SHIFT> PLOT will send the digital storage waveform(s) that are displayed, as well as the graticule and bezel (if GRAT ILLUM is on), and the crt readout (if READOUT is on) to the plotter.

To use or check the plot feature, connect the Digital Plotter to the 494P with a IEEE STD 488 (GPIB) cable and perform the following:

(1) Set the corners of the plot for a 3:2 aspect ratio for Tektronix plotters, or 6:5 for the Hewlett-Packard plotter. The Digital Plotter must be in the Listen Only mode and the 494P must be in either the TALK ONLY or TALK/LISTEN ONLY mode (appropriate switches on the rear panel GPIB ADDRESS switch, closed or in the 1 position).

(2) Set the Plotter Interface switches as follows:

TEKTRONIX 4662 or 4662 Option 31 (rear panel)

A = 0, 1, 8, or 9
B = C or D
C = X (don't care)
D = X (don't care)

TEKTRONIX 4663

Interface Select = 1 if Option 04 or 2 if Option 01
Initial Command/Response Format = 5
Interface Mode = Listen Only

HEWLETT-PACKARD

Address = 31

(3) Select the plotter type by pressing <SHIFT> SAVE A, on the 494/494P, and answer the type plotter question on the crt message. The selection is stored in battery-powered memory and need not be selected again unless the type plotter is changed. To use a 4663 emulating a 4662, select 0 (4662) for a one-pen configuration or select 1 (4662 Option 31) for a two pen configuration. Select the display and the information that you wish to plot.

The zero level for a B−SAVE A waveform is assummed to be the graticule center line. (Switches within the instruument can set the zero level, contact your service

personnel for this change.) If you desire to shift the zero level for the PLOT only, press <SHIFT>, B–SAVE A, and enter the desired level in display units (25 is bottom graticule line, 25 units/div is required). This zero level is retained in non-volatile memory; however, it is not related to the display zero level since the processor has no way of determining the internally set zero level for the crt display or no way of changing it.

(4) Press <SHIFT> PLOT. During the plot operation, the front panel controls are operational except STORE DISP, RECALL, and AUTO PEAK; so the instrument can be used for other measurements.

This completes the operational check of the front panel controls and selectors.

2. Check Reference Oscillator Accuracy

Reference oscillator accuracy is not a performance requirement: however, it must be checked so the center frequency accuracy can be verified. Since the Calibrator is locked to the reference oscillator this procedure verifies accuracy by counting the frequency of the calibrator signal. Allow 30 minutes or more warm-up time for the oscillator to stabilize before proceeding with this check.

a. Connect the counter to the CAL OUT. Set the counter display resolution to 1 Hz.

b. Check — Frequency of the calibrator must be 100 MHz ±10 Hz.

c. Disconnect the counter from the CAL OUT connector.

3. Check Counter Accuracy ±[(10 + 2N)Hz + 1LSD]

a. Set the FREQUENCY to 500 MHz and the FREQ SPAN/DIV to 20 kHz, via the Data Entry keyboard. Activate 10 dB/DIV Vertical Display, set the TIME/DIV to AUTO, REF LEVEL −30 dBm, and activate AUTO RESOLN.

b. Apply the CAL OUT signal to the RF INPUT and center the 500 MHz marker under the dot marker.

c. Press <SHIFT> COUNT RESOLN and enter 1 Hz via the Data Entry keyboard.

d. Press COUNTER and note that the error over several counts does not exceed 13 Hz.

e. Change FREQ SPAN/DIV to 500 kHz and repeat part d.

f. Press <SHIFT> COUNT RESOLN and enter 1 kHz for a counter resolution of 1 kHz.

g. Press COUNTER and note that the error over several counts does not exceed 1 kHz.

h. Change the FREQ SPAN/DIV to 200 kHz and repeat part g.

i. Set the FREQUENCY to 1.8 or 1.7 GHz and repeat the counter accuracy check for this end of the band.

4. Check Counter Sensitivity

Counter should count a signal that is 20 dB above the noise floor and above a level that is 60 dB down from the REF LEVEL.

a. Test equipment setup is shown in Figure 4-3. Apply the CAL OUT signal through 1 dB and 10 dB step attenuators to the RF INPUT.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 1 MHz, RESOLUTION BANDWIDTH to 1 MHz, REF LEVEL to 0 dBm, and activate NARROW Video Filter.

c. Adjust CENTER FREQUENCY to position the peak of the 100 MHz signal directly below the dot marker. Add attenuation to reduce the signal amplitude until it is 20 dB above the noise floor.

d. Press <SHIFT> COUNT RESOLN and enter 1 Hz via the Data Entry keyboard.

e. Press COUNTER and note that the counter is counting the signal with the accuracy noted in step 3.

f. Change FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 Hz, REF LEVEL to −30 dBm, and activate WIDE Video Filter.

g. Increase the attenuation until the signal amplitude decreases to a level that is is 60 dB below the REF LEVEL and adjust CENTER FREQUENCY to place the signal directly under the dot marker.

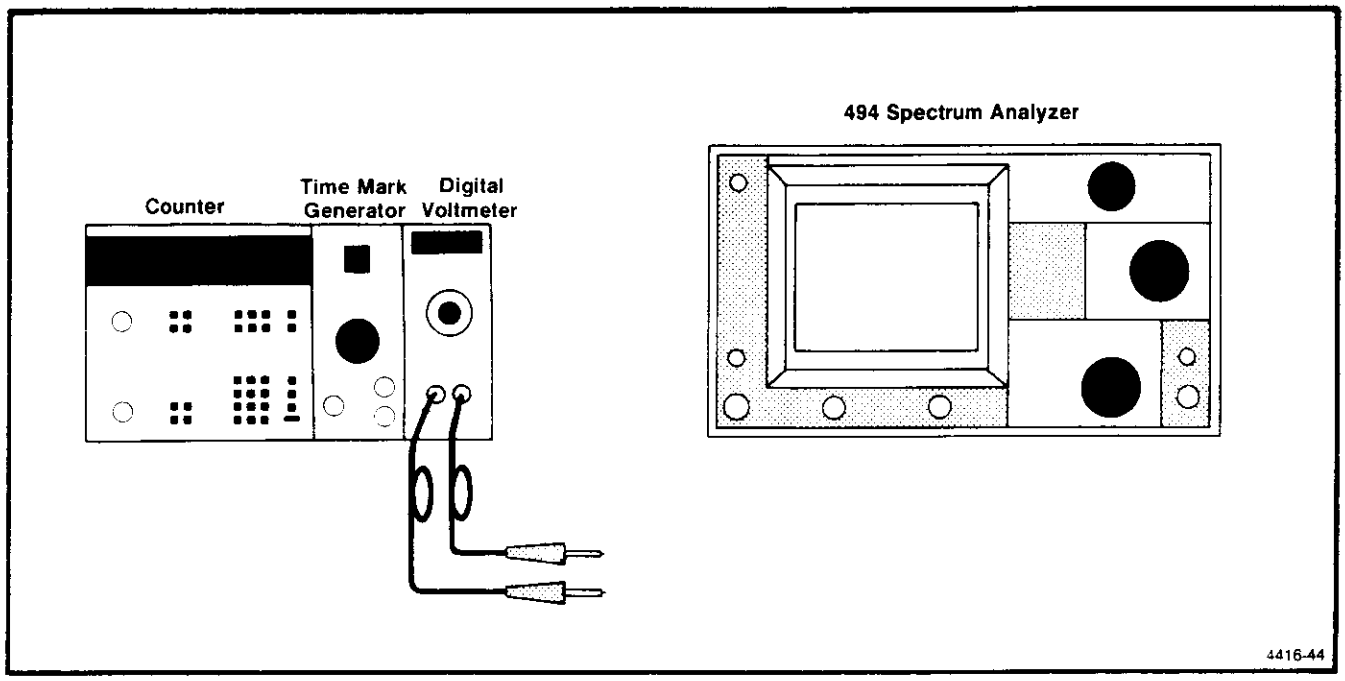


Figure 4-3. Test equipment setup for checking center frequency accuracy.

h. Press COUNTER and note that the counter is counting the signal and the count is accurate.

i. Deactivate COUNTER and WIDE Video Filter. Activate AUTO RESOLN and switch FREQ SPAN/DIV to 200 kHz.

5. Check Center Frequency Accuracy

This is a two part procedure; part 1 checks center frequency accuracy without the 1st LO phase locked, part 2 checks accuracy with the 1st LO phase locked. A front panel CAL should be done before performing this check.

Center frequency accuracy is a function of how accurate the center frequency is set between sweeps and the amount of frequency drift during the sweep. Frequency drift can be significant during the first 30 minutes after turn-on or when the ambient temperature changes. With a span/div of 50 Hz and 30 Hz resolution bandwidth, the sweep rate is slow enough that frequency drift can be noted if the warmup time is insufficient or the ambient temperature is changing. "N" is the 1st LO harmonic number used for the first conversion (refer to IF Frequency, LO Range, and Harmonic Number, in Specifications section for value of N, or activate the HELP message for the (down) FREQUENCY RANGE).

This check is dependent on the performance of the reference oscillator and the counter accuracy (see steps 2 and 3).

Part 1 — 1st LO not phase locked

Accuracy for bands 1 & 5-12 with Span/Div >200 kHz, and bands 2-4 with Span/Div >100 kHz: ±[(20% of the Span/Div or Resoln Bandwidth, whichever is greater) + (CF x reference frequency error) + (N x 15 kHz)] A settling time of 1 s/GHz change in center frequency divided by "N" must be allowed before checking accuracy. A front panel CAL should be done before proceeding with this check.

(1) Equipment setup is shown in Figure 4-3

(2) Apply the output of the comb generator to the RF INPUT. Set the FREQUENCY to 500 MHz and the FREQ SPAN/DIV to 210 kHz, via the Data Entry keyboard. Activate AUTO RESOLN, 10 dB/DIV, and set REF LEVEL to +20 dBm

(3) Press COUNT→CF and change the RESOLUTION BANDWIDTH to 10 kHz.

(4) Note that the signal is within ±[(20% of Span/Div or Resoln Bandwidth) + (N X 15 kHz)] or ±57 kHz (±1.35 minor div) of the dot marker.

(5) Set the FREQUENCY to 1.0 GHz and RESOLUTION BANDWIDTH to 1 MHz.

(6) Press COUNT→CF and change the RESOLUTION BANDWIDTH to 10 kHz.

(7) Check — that the signal is within 57 kHz of the dot marker.

(8) Repeat the procedure to check accuracy at a center frequency of 1.5 GHz (the upper end of band 1).

(9) Using the above procedure and Table 4-2, check center frequency accuracy to 21 GHz for those span/div settings in which the 1st LO is not phase locked.

Part 2 — 1st LO phase locked

Accuracy for bands 1 & 5-12 with Span/Div ≤200 kHz and bands 2-4 with Span/Div ≤100 kHz: ± [(20% of the Span/Div or Resoln Bandwidth, whichever is greater) + (CF x reference frequency error) + (2N + 25)]Hz.

(1) Apply the CAL OUT signal to the RF INPUT. Press <SHIFT> FREQ and enter 100 MHz via the Data Entry keyboard. Set FREQ SPAN/DIV to 50 Hz and the REF LEVEL to −20 dBm. Activate AUTO RESOLN and 2 dB/DIV, then adjust the REFERENCE LEVEL so the top of the signal is below the dot marker.

(2) Check 100 MHz center frequency accuracy by measuring the deviation of the 100 MHz signal from the dot marker. Error must not exceed ±(20% of the span/Div) + (25 + 2N) or ±37 Hz (±3.7 minor division).

(3) Repeat this procedure to check the center frequency accuracy to 1.8 GHz in 100 MHz increments. Adjust the REF LEVEL as necessary to observe the comb of 100 MHz markers at the upper end of the range.

6. Check Center Frequency Drift or Stability

Drift is 50 Hz or less per minute of sweep time, with 1st LO phase locked (FREQ SPAN/DIV 200 kHz or less for bands 1 & 5-12 and 100 kHz or less for bands 2-4) — after 1 hour of warmup, and within a stable ambient temperature.

a. With the Calibrator signal applied to the RF INPUT, set the FREQUENCY to 100 MHz, TIME/DIV to AUTO, FREQ SPAN/DIV at 50 Hz, RESOLUTION BANDWIDTH at 30 HZ, Vertical Display of 2 dB/DIV, and REF LEVEL of −23 dBm. Switch VIEW A and VIEW B on.

b. Adjust the CENTER FREQUENCY control so one side of the signal intersects the sixth division graticule line, from the left edge, then press SINGLE SWEEP. Activate SAVE A to save the display.

Table 4-2
CENTER FREQUENCY ACCURACY CHECK POINTS FOR UNLOCKED 1st LO

Band	N	Center Freq	Freq Span/Div	Maximum Error	Error Minor Div
1	1	0.5 GHz	210 kHz	±57 kHz	±1.35
		1.0 GHz	210 kHz	±57 kHz	±1.35
		1.5GHz	210 kHz	±57 kHz	±1.35
2	1	2.0 GHz	110 kHz	±37 kHz	±1.35
		3.0GHz	110 kHz	±37 kHz	±1.35
		4.0 GHz	110 kHz	±37 kHz	±1.35
		5.0GHz	110 kHz	±37 kHz	±1.35
3	1	6.0 GHz	110 kHz	±37 kHz	±1.35
		6.5GHz	110 kHz	±37 kHz	±1.35
		7.0 GHz	110 kHz	±37 kHz	±1.35
4	3	7.5 GHz	110 kHz	±67 kHz	±1.35
		9.5 GHz	110 kHz	±67 kHz	±1.35
		11.5GHz	110 kHz	±67 kHz	±1.35
		13.5 GHz	110 kHz	±67 kHz	±1.35
		15.5GHz	110 kHz	±67 kHz	±1.35
		17.5 GHz	110 kHz	±67 kHz	±1.35
		18.0GHz	110 kHz	±67 kHz	±1.35
5	3	18.5 GHz	210 kHz	±87 kHz	±1.35
		20.0GHz	210 kHz	±87 kHz	±1.35
		21.0 GHz	210 kHz	±87 kHz	±1.35

c. Select the NARROW Video Filter and press SINGLE SWEEP again to start the sweep. The sweep will now run at a 10 s/div rate.

d. Note the frequency difference between the two displays, at the 6th graticule line as Δ f.

e. Check — the frequency drift rate/minute. Drift is (300 x Δ f) / (250 + Δ f) per minute. Drift rate must not exceed 50 Hz/min.

7. Check Residual FM

Within (7 kHz)N over 20 ms, with FREQ SPAN/DIV greater than 200 kHz, and within (10 + 2 N) Hz over 20 ms, with FREQ SPAN/DIV of 200 kHz or less)

a. With the Calibrator signal applied to the RF INPUT, set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 1 MHz, RESOLUTION BANDWIDTH to 100 kHz, Vertical Display to 2 dB/DIV, and REF LEVEL to −23 dBm.

b. Press <SHIFT> FREE RUN. A message "FREQUENCY CORRECTIONS DISABLED" will come on screen, which indicates that the 1st LO synthesis and phase lock are disabled; this is normal. It is now possible to switch the FREQ SPAN/DIV to narrower spans with phase lock disabled.

c. Decrease the FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 kHz and keep the 100 MHz calibrator signal centered on screen with the CENTER FREQUENCY control.

d. Switch the Vertical Display to LIN. Position the signal so the slope (horizontal versus vertical excursion) of the response can be determined as illustrated in Figure 4-4A. It may help to determine slope by switching VIEW B off and using SAVE A and VIEW A to freeze the display at a convenient point on the graticule for measurement. Slope should calculate to approximately 8 kHz/division.

e. If SAVE A was used in step d, de-activate SAVE A and VIEW B. Activate ZERO SPAN, set TIME/DIV to 20 ms, and adjust CENTER FREQUENCY control to position the display near center screen as shown in Figure 4-4B. Use SAVE A to freeze the display for ease in measuring the FM. The peak-to-peak amplitude of the display per any horizontal division, scaled to the vertical deflections according to the slope estimated in part d is the FM. Residual FM must not exceed 7 kHz for 20 ms or 7 kHz/division.

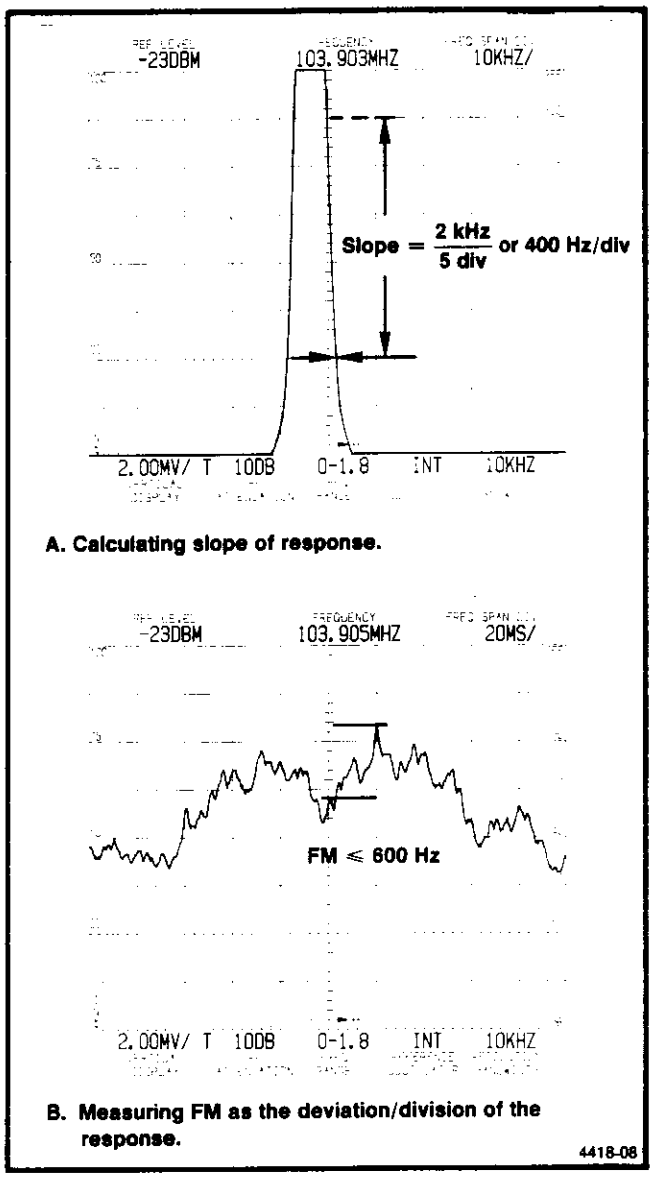


Figure 4-4. Typical display that illustrates how residual FM is measured.

f. Press <SHIFT> FREE RUN to re-enable the phase lock, set the FREQUENCY to 100 MHz and switch the TIME/DIV to AUTO. Reduce the FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 100 Hz.

g. Adjust the CENTER FREQUENCY control to position the signal so its slope can be determined. Again, it will be easier if you use SINGLE SWEEP and SAVE A to freeze the display at a convenient position on the graticule.

h. Deactivate SAVE A and SINGLE SWEEP and switch the TIME/DIV to 20 ms. Activate ZERO SPAN and position the display near center screen so the vertical excursions per horizontal division (20 ms) can be measured. Residual FM must not exceed 12 Hz within any one horizontal division.

8. Check Frequency Span/Div Accuracy ±5% of the selected span/div

Span accuracy is checked by noting the displacement of calibrated markers from their respective graticule line over the center eight divisions of the screen. The frequency span/div accuracy is checked, for all FREQ SPAN/DIV settings on band 1, at 100 kHz/Div on band 2, (2nd LO check) and at 500 MHz/Div on band 4. The accuracy of the 1 GHz, 5 GHz, and 10 GHz span/div selections, for the upper bands, is directly related to the 100 MHz/div and 200 MHz/div selections: therefore, they are not included in this procedure.

FREQUENCY SPAN/DIV range is 50 Hz to 200 MHz for the 0 to 7.1 GHz bands, increasing in a 5, 1, 2, 5 sequence to 10 GHz for bands 11 and 12. Selection is in a 5, 2, 1 sequence with the FREQUENCY SPAN/DIV control and by two significant digits with the Data Entry keyboard.

a. Equipment setup is shown in Figure 4-5 .

b. Set the FREQUENCY to 1 GHz, FREQ SPAN/DIV to 200 MHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at 0.5 s, REF LEVEL to −30 dBm, and Vertical Display to 10 dB/DIV.

c. Apply the CAL OUT signal to the RF INPUT and adjust the FREQUENCY to align the 100 MHz markers so the 200 MHz/div accuracy can be measured over the center eight divisions of the display (two markers per division). It may be necessary to change the REF LEVEL to obtain adequate markers. Maximum deviation (see Figure 4-6) must not exceed 10 MHz (0.25 minor divisions).

d. Change the FREQ SPAN/DIV to 100 MHz and check the span/div accuracy. Error must not exceed 5% of the FREQ SPAN/DIV or 5 MHz.

e. Remove the CAL OUT signal to the RF INPUT and apply the output of the Microwave Comb Generator, as shown in Figure 4-5. Set the FREQUENCY to 10 GHz, (band 4, 5.4 to 18 GHz) FREQ SPAN/DIV to 500 MHz, RESOLUTION BANDWIDTH to 100 kHz, and REF LEVEL to −10 dBm. Peak the response with the MANUAL PEAK control and adjust REF LEVEL for the best marker definition. It may also help to adjust the CENTER FREQUENCY for better marker definition.

f. Tune a marker to center screen then check the accuracy over the center eight divisions of the display. Deviation must not exceed ±25 MHz.

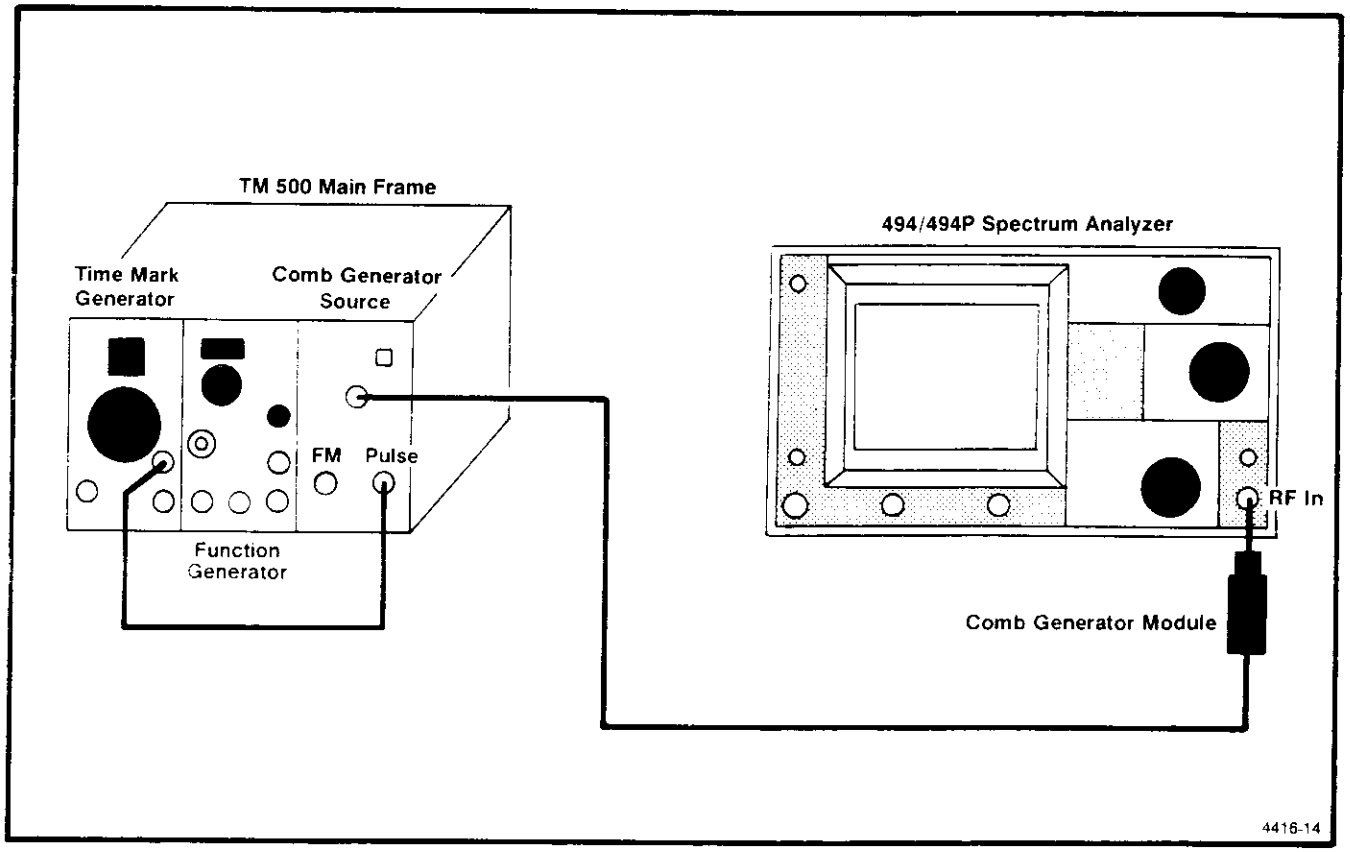


Figure 4-5. Test equipment setup for checking frequency span/div and sweep time/div accuracy.

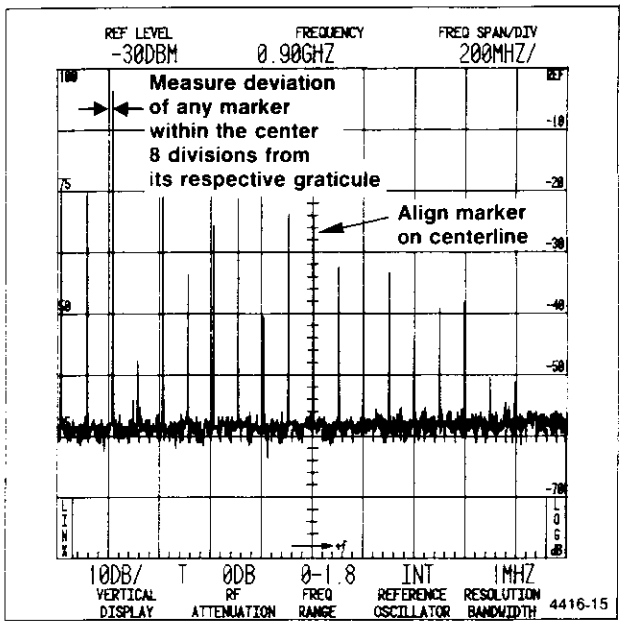


Figure 4-6. Typical marker display that shows how span/div accuracy is measured.

g. Set the FREQUENCY to 2.0 GHz, FREQ SPAN/DIV to 100 kHz, RESOLUTION BANDWIDTH to 1 kHz, TIME/DIV to 50 ms, and REF LEVEL to −20 dBm.

h. Modulate the Comb Generator signal with 10 μs markers, from the Time Mark Generator, by applying the Marker Output to the Pulse Input of the Comb Generator as shown in Figure 4-5. Adjust the MANUAL PEAK control for optimum marker definition.

i. Check FREQ SPAN/DIV accuracy. Error must not exceed ±5 kHz.

j. Remove the Comb Generator signal from the RF INPUT and connect the Marker Output of the Time Mark Generator to the RF INPUT. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 50 MHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to −20 dBm, and apply 20 ns time markers from the Time Mark Generator.

k. Adjust the REF LEVEL for the best marker definition and the CENTER FREQUENCY to align the markers so span/div accuracy can be checked for the 50 MHz/div.

l. Reduce the FREQ SPAN/DIV to 20 MHz, CENTER FREQUENCY to 100 MHz, and apply 50 ns (20 MHz) markers.

m. Check the 20 MHz FREQ SPAN/DIV accuracy.

n. Repeat the procedure and check the FREQ SPAN/DIV accuracy from 10 MHz down to 200 kHz. Use Table 4-3 as a guide to relate time markers to FREQ SPAN/DIV settings. Reduce RESOLUTION BANDWIDTH and CENTER FREQUENCY as each setting is checked to maintain marker amplitude and definition.

o. Change the TIME/DIV to 0.5 s and RESOLUTION BANDWIDTH to 100 Hz. Repeat the above procedure to check the 100 kHz to 10 kHz FREQ SPAN/DIV selections.

p. Set the FREQUENCY to 100 kHz, RESOLUTION BANDWIDTH to 30 Hz, TIME/DIV to 1 s and REF LEVEL to 0 dBm. Repeat the above procedure to check the 5 kHz to 200 Hz FREQ SPAN/DIV selections.

q. Activate the 2 dB/DIV Vertical Display mode, increase REF LEVEL to approximately −28 dBm. Repeat the procedure to check the 100 Hz and 50 Hz FREQ SPAN/DIV selections.

Table 4-3
SPAN/DIV VERSUS TIME MARKERS FOR SPAN/DIV ACCURACY CHECK

FREQUENCY SPAN/DIV	Time Mark Generator Marker Output
20 MHz	50 ns
10 MHz	.1 μs
5 MHz	.2 μs
2 MHz	.5 μs
1 MHz	1 μs
500 kHz	2 μs
200 kHz	5 μs
100 kHz	10 μs
50 kHz	20 μs
20 kHz	50 μs
10 kHz	.1 ms
5 kHz	.2 ms
2 kHz	.5 ms
1 kHz	1 ms
500 Hz	2 ms
200 Hz	5 ms
100 Hz	10 ms
50 Hz	20 ms

9. Check Time/Div Accuracy (accuracy within 5% of time selected)

a. Test equipment setup is the same as that required for step 8.

b. Apply the Marker Output from the Time Mark Generator directly to the RF INPUT. Apply the Trigger Output to the 494/494P HORIZ/TRIG connector on the back panel.

c. Activate ZERO SPAN. Set the RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL at 0 dBm, TIME/DIV to 50 ms, MIN RF ATTEN to 20 dB, FREQUENCY to 1 MHz and the Triggering mode to EXT.

d. Apply 50 ms time markers. Adjust CENTER FREQUENCY, if necessary, to display the markers on the time domain display (see Figure 4-7).

e. Use the horizontal position control to align a marker on the 1st graticule line, then check the displacement of markers from their respective positions over the center eight divisions. Individual marker displacement must not exceed 5% or 2 minor divisions.

f. Check the accuracy of the 50 ms to 2 ms TIME/DIV settings,then the postion and note the displacement as described in part "e" of this step.

g. Deactivate the VIEW A and VIEW B mode. Change the RESOLUTION BANDWIDTH to 100 kHz, the Vertical Display to 2 dB/DIV, and the REF LEVEL to −10 dBm.

h. Check the accuracy of the 1 ms to 20 μs TIME/DIV selections.

10. Check Pulse Stretcher

This is an operational check only.

a. With the equipment setup the same as step 9, apply 1 ms time marks, from the Time Mark Generator, to the RF INPUT. Set the TIME/DIV to 0.1 ms, RESOLUTION BANDWIDTH to 100 kHz, Vertical Display to 10 dB/DIV, and REF LEVEL to 0 dBm. Set the FREQUENCY to 2.0 MHz, switch VIEW A and VIEW B off, and activate ZERO SPAN.

b. Activate PULSE STRETCHER and note that this mode extends the fall-time of the markers.

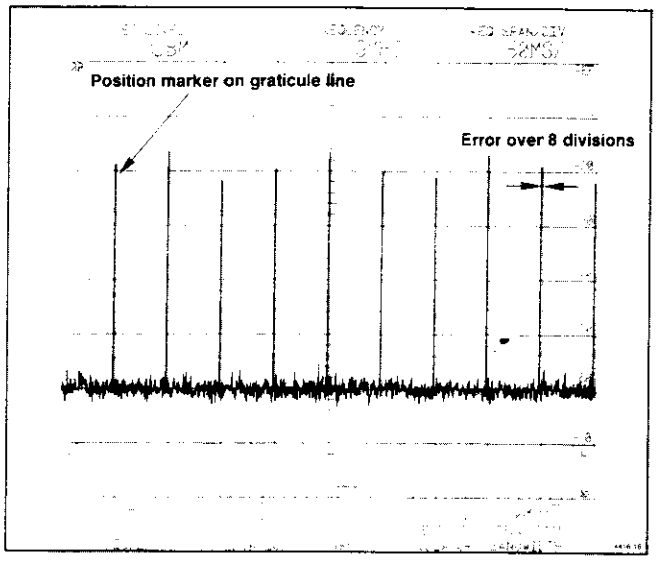


Figure 4-7. Typical display to illustrate how time/div accuracy is measured.

c. Remove the Time Mark Generator outputs to the RF INPUT and HORIZ/TRIG inputs of the 494/494P. Deactivate PULSE STRETCHER, ZERO SPAN and return the MIN RF ATTEN to 0 dB.

11. Check Resolution Bandwidth and Shape Factor

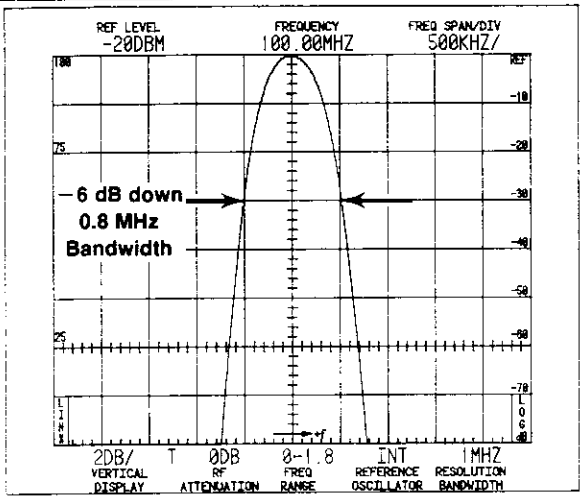
Bandwidth is within 20% of the 1 MHz to 30 Hz range, in decade steps to 100 Hz, then 30 Hz; shape factor is 7.5:1 or less to 100 Hz, and 15:1 or less for the 30 Hz bandwidth.

a. With the Calibrator output applied to the RF INPUT and the FREQUENCY set to 100 MHz, set the REF LEVEL to −20 dBm, FREQ SPAN/DIV to 500 kHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at AUTO, and Vertical Display to 2 dB/DIV. Activate MIN NOISE.

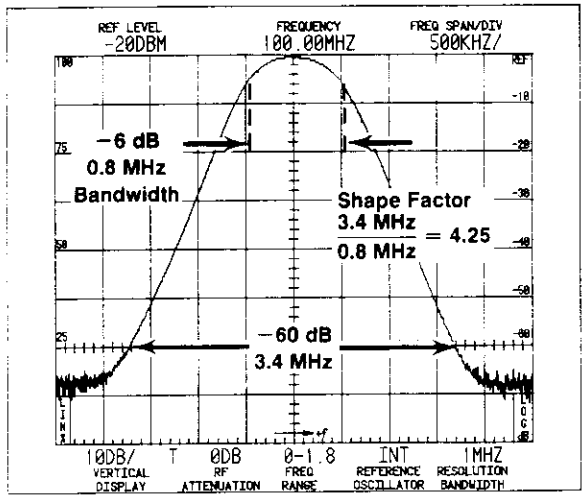
b. Measure the 6 dB down bandwidth (see Figure 4-8A). Bandwidth should equal 1 MHz ±200 kHz.

c. Change the Vertical Display to 10 dB/DIV and measure the 60 dB down bandwidth (see Figure 4-8B).

d. Calculate the shape factor as the ratio of −60 dB/−6 dB bandwidths (see Figure 4-8). Shape factor should equal 7.5:1 or less.



A. Measuring 6dB down bandwidth.



B. Measuring 60dB down bandwidth and computing shape factor.

4418-07

Figure 4-8. Typical display to illustrate how response bandwidth and shape factor are determined.

e. Change the RESLOLUTION BANDWIDTH to 100 kHz and the FREQ SPAN/DIV to 100 kHz.

f. Check the resolution bandwidth and shape factor of the 100 kHz filter by repeating the above process.

g. Repeat the process to check the resolution bandwidth and shape factor for the 10 kHz, 1 kHz, 100 Hz, and 30 Hz filters. Shape factor should equal 7.5:1 for all except the 30 Hz filter which is 15:1 or less.

NOTE

Because of residual FM'ing (10 + 2N)Hz in 20 ms, The bandwidth of the 30 Hz filter cannot be measured to ±20% with the above procedure; and additional 12 Hz error must be included with the specification.

12. Check Noise Sidebands

Noise sidebands are −75 dBc or more at 30 times the resolution bandwidth offset, fundamental mixing; and −70 dBc or more for 100 Hz or less resolution bandwidths.

a. Set FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, and REF LEVEL to −20 dBm. Activate 10 dB/DIV, AUTO RESOLN, and WIDE Video Filter.

b. Apply the CAL OUT signal to the RF INPUT. Change REF LEVEL to −40 dBm to position the signal peak 20 dB above the reference line.

c. Check the amplitude of the noise sidebands 30 times the resolution bandwidth away from the signal (Figure 4-9). Noise sidebands should be 75 dB or more below the peak signal level or 55 dB below the top of the screen.

d. Decrease the FREQ SPAN/DIV to 1 kHz and the RESOLUTION BANDWIDTH to 100 Hz.

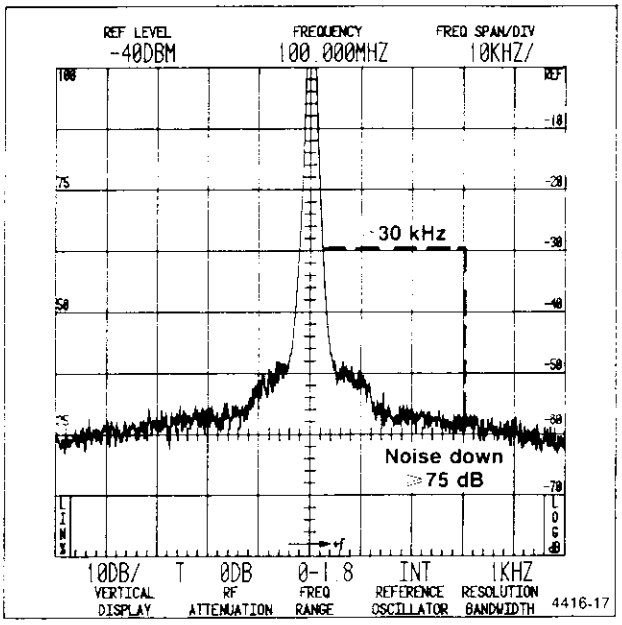


Figure 4-9. Typical display showing how to measure noise sidebands.

e. Check the amplitude of the noise sidebands 3 kHz away from the signal. Noise sidebands should be 70 dB below the signal level or 50 dB below the top of the screen.

13. Check Calibrator Output −20 dBm ±0.3 dB at 100 MHz

Three procedures for measuring output level are described: vector voltmeter, power meter, and comparison between an accurate −20 dBm source and the Calibrator output.

Vector Voltmeter Method

(1) Test equipment setup is shown in Figure 4-10.

(2) Terminate the voltmeter probe with a 50 Ω feedthrough termination and then connect the terminated probe to the CAL OUT connector

(3) Set the vector voltmeter frequency to 100 MHz.

(4) Check - for an rms reading between 21.11 mV and 22.69 mV. (22.36 mV rms, across 50 Ω, is −20 dBm.)

Power Meter Measurement

(1) Test equipment setup is shown in Figure 4-10.

(2) Connect the power meter sensor through a low-pass filter (≥40 dB, at 200 MHz, to remove harmonics of the fundamental) to the CAL OUT connector.

NOTE

Insertion loss of the filter with pads, measured at 100 MHz, must be determined to within 0.05 dB. To ensure a 50 Ω match, use approximately 3 dB minimum-loss matching pads (attenuator) on both sides of the filter.

(3) Note the power reading. Reading, plus the loss through the filter and pads, must equal −20 dBm, ±0.3 dB.

Signal Substitution Method

NOTE

A power meter is used to verify the output level of the reference signal. Harmonics of the signal source must be greater than 40 dB down.

(1) Apply a 100 MHz signal from a signal source (signal generator) through a 3 dB attenuator to the power meter. Adjust the output level for −20 dBm reading on the power meter.

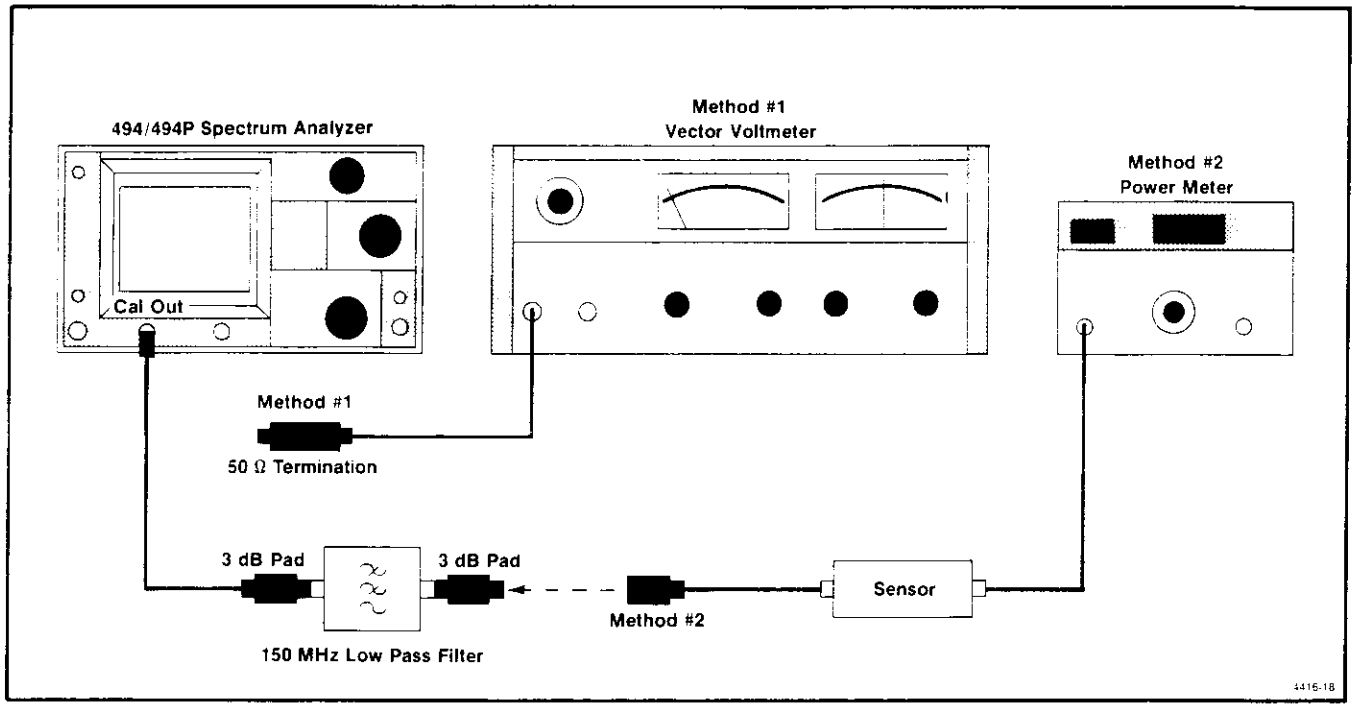


Figure 4-10. Test equipment setup for checking the calibrator output level.

(2) Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz,RESOLUTION BANDWIDTH to 1 MHz, and set the REF LEVEL to −18 dBm. Set TIME/DIV to AUTO and turn the PEAK/AVERAGE control fully clockwise

(3) Disconnect the meter and (using the same instrument cable and attenuator) apply the calibrated reference signal to the RF INPUT.

(4) Set the Vertical Display factor to the Δ A mode by pressing FINE. Adjust the REF LEVEL so the top of the signal is on a graticule line near the top of the screen. Reset the REF LEVEL to 0.00 dB by pressing FINE twice. If desired, store the display by activating SAVE A.

(5) Remove the reference signal and apply the CAL OUT signal to the RF INPUT.

(6) Adjust the REF LEVEL until the signal is the same amplitude as the reference established in part 4. Note the displacement, of the CAL signal from the reference, as the Δ A readout.

An alternate method to measure the difference is as follows: Decrease the RESOLUTION BANDWIDTH to 100 kHz, activate B−SAVE A, and note the displacement between the CAL signal and the reference. Displacement must not exceed 0.3 dB.

14. Check Frequency Response

Response, about the midpoint of the two extremes, is: ±1.5 dB from 50 kHz to 1.8 GHz; ±2.0 dB from 10 kHz to 1.86 Hz; ±2.5 dB from 1.7 to 7.1 GHz; ±3.5 dB from 5.4 to 18 GHz; and ±5.0 dB from 15 to 21 GHz. Response with respect to 100 MHz: ±3.5 dB from 1.7 to 7.1 GHz; ±4.5 dB from 5.4 to 18 GHz; and ±6.5 dB from 15.0 to 21 GHz.

Frequency response is the peak-to-peak variation of the displayed amplitude over a specified center frequency range, measured at the center frequency. It is measured with 10 dB of RF attenuation, with Peaking optimized, for those bands that are applicable, for each center frequency setting. Response includes the effect of input vswr, mixing mode (N), gain variation, and preselector or mixer. Digital storage typically increases errors by 0.5%.

Accurate measurement requires many small incremental checks across the frequency range. The response at each check point, above band 1, should be peaked with MANUAL PEAK or by activating the AUTO PEAK mode. When checking the external mixer bands the signal must be identified as a true response and peaked.

If your instrument is the rackmount version, with semi-rigid cables to the back panel (Option 31), frequency response may degrade at the higher frequency end (see Rackmount/Benchtop Version, Options section for details).

NOTE

Loss of signal through interconnecting cables becomes significant above 1 GHz; therefore, short (25 inch or less) semi-rigid cable with precision fittings to interconnect the test equiment should be used. Precise matching terminations and power dividers are also used to minimize reflections.

To expedite the measurement, this procedure uses a leveled output sweep oscillator rather than incremental checks. Digital storage is also used to provide a complete display of the swept frequency. VIEW A, VIEW B and MAX HOLD are reactivated for each sweep.

a. Test equipment setup is shown in Figure 4-11. Set the FREQUENCY to 5 MHz, FREQ SPAN/DIV to 1 MHz, TIME/DIV to 20 ms, REF LEVEL to 0 dBm, and MIN RF ATTEN to 30 dB. Activate 1 dB/div and AUTO RESOLN.

b. Apply the output of a constant level and calibrated 10 kHz to 10 MHz Signal Generator to the RF INPUT of the 494/494P. Set the generator frequency to 100 kHz and its output for about −10 dBm.

c. Adjust the REF LEVEL so the amplitude of the 100 kHz signal is about half screen, in the 2 dB/DIV mode. Activate VIEW A, SAVE A, and MAX HOLD.

d. Slowly tune the Signal Generator frequency from 10 kHz to 10 MHz, monitoring the output to ensure it remains constant. Note the frequency response (amplitude deviation above and below the average). Frequency response or amplitude deviation must not exceed ±1.5 dB from 50 kHz to 10 MHz or ±2.0 dB from 10 kHz to 10 MHz. (See Figure 4-12 for the average level.)

e. Replace the 10 kHz to 10 MHz signal source with a 0.01 to 2.4 GHz sweep oscillator and connect the test equipment as shown in Figure 4-13. The output of the Sweep Generator is applied through a 3 dB attenuator and high performance coaxial cable to a power divider. Connect one output of the power divider to the RF INPUT of the 494/494P and the other output to the sensor for the power meter or to the ALC input of the sweep oscillator.

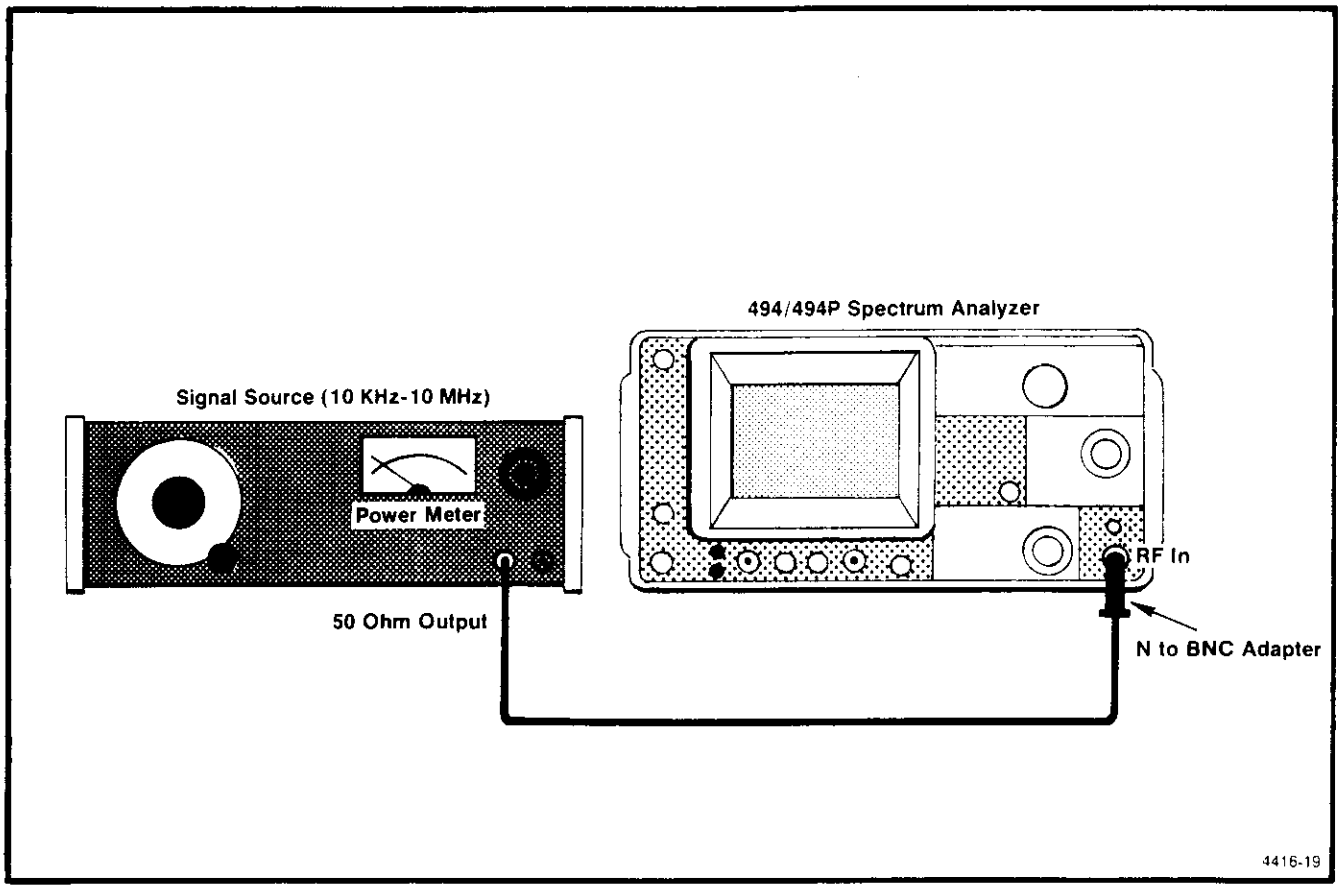


Figure 4-11. Test equipment setup for measuring 10 kHz to 10 MHz frequency response.

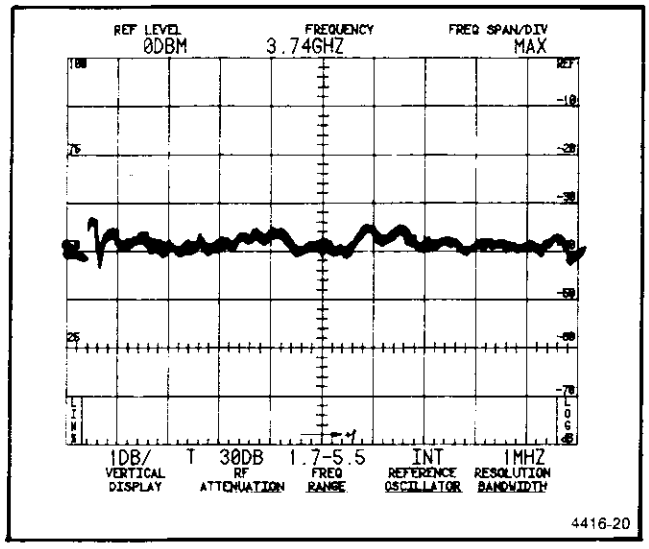


Figure 4-12. Display showing frequency response pattern from a sweeping source.

f. Change the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to approximately 1.0 GHz. On the Sweep Generator, select a 1 GHz cw marker and adjust the output for a −6 dBm reading on the power meter. With the Vertical Display in the 2 dB/DIV mode, adjust the REF LEVEL so the signal amplitude is about half screen.

g. Change the Sweep Generator sweep mode to Automatic Internal Sweep and set the Sweep Time to 100 s for its slowest sweep time.

h. Check the frequency response over the 10 MHz to 1.8 GHz span. Deviation must not exceed ±1.5 dB (Figure 4-12).

i. Change the FREQUENCY to 2.0 GHz and the FREQ SPAN/DIV to 100 MHz. Switch the Sweep Generator CW Marker on, and set it to 2.0 GHz. Peak the signal response of the 494/494P with the MANUAL PEAK control, or activate AUTO PEAK.

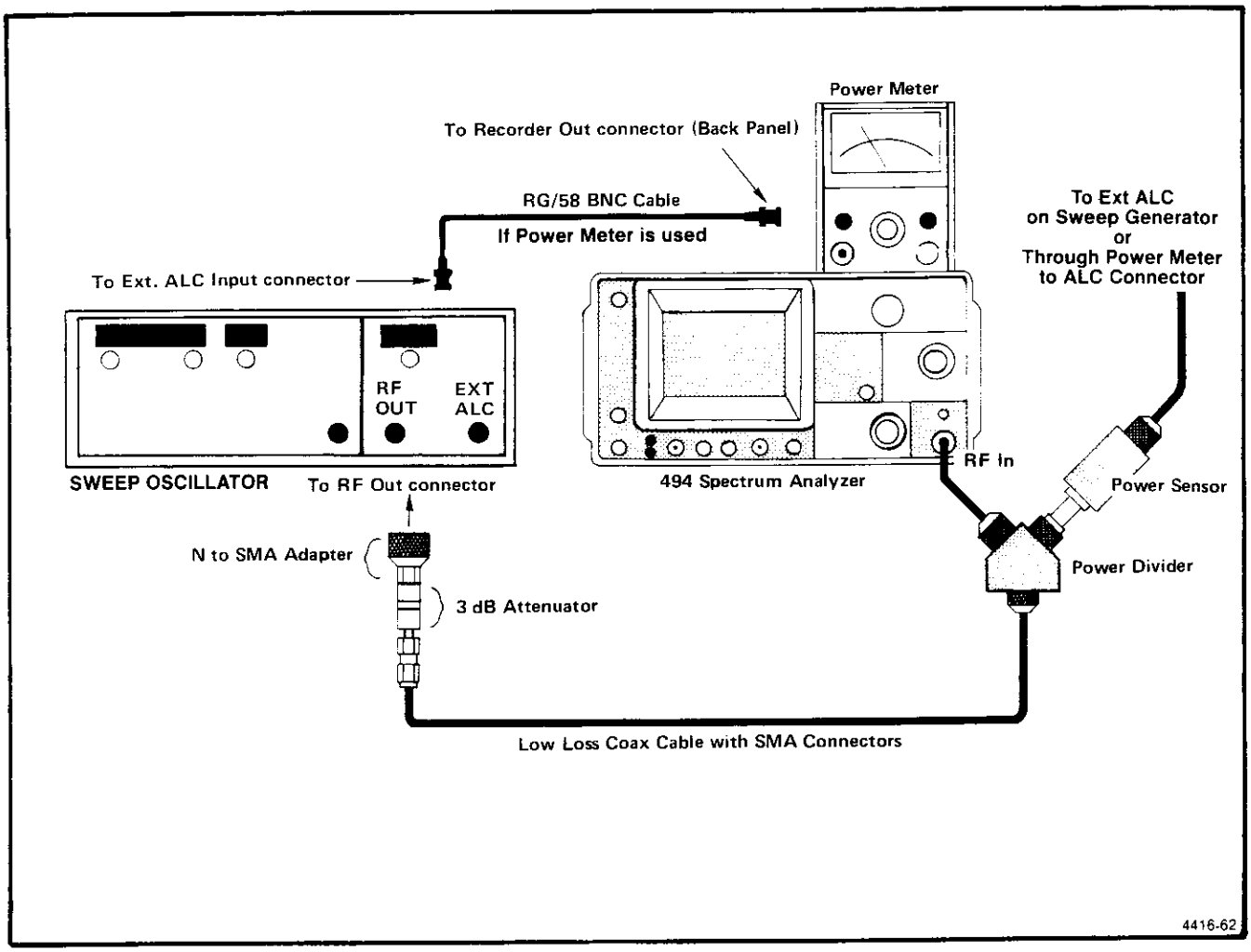


Figure 4-13. Test equipment setup for measuring .01 to 21 GHz frequency response.

j. Return the Sweep Generator to its Sweep mode and set the Start/Stop markers for 1.5 and 2.5 GHz. Sweep the 1.7 to 2.5 GHz span for Band 2 and note the frequency response. Frequency response or deviation must not exceed ±2.5 dB.

NOTE

If any segment or portion of the span fails to meet the ±2.5 dB specification, set the FREQUENCY to the center of this portion; apply a cw marker at this center frequency and re-peak with the MANUAL PEAK or AUTO PEAK mode. Decrease the FREQ SPAN/DIV to display that portion and then recheck the frequency response for this portion.

k. Replace the 0.01 to 2.4 GHz sweep source with a sweep oscillator that covers the frequency range to 21 GHz. Connect the test equipment as shown in Figure 4-13. On the RF plug-in, switch the ALC to Mtr position and connect a coaxial cable between the Recorder Output of the power meter and the Ext ALC Input of the plug-in unit. Decrease the Power Level to approximately −6 dBm then adjust the Gain for stable operation (output stops oscillating).

l. Set the FREQ SPAN/DIV to 200 MHz and the FREQUENCY to 4.0 GHz. Re-peak the response with the peaking controls, then sweep the upper portion of band 2 and check frequency response. If necessary, recheck those portions that do not meet specification after peaking the response at the center of those portions of the frequency spectrum.

m. Increase the FREQUENCY RANGE to the 3.0 to 7.1 GHz band. Tune the CENTER FREQUENCY to approximately 5.0 GHz. Apply a 5.0 GHz cw marker and peak the response. Activate MAX SPAN and check the frequency response by sweeping the 3.0 to 7.1 GHz frequency range. It may be necessary, if the response does not meet the ±2.5 dB performance, to again peak the response at the

center of those portions that do not meet specifications and recheck frequency response in smaller segments.

n. Repeat the foregoing procedure to check the response of the remaining bands to 21 GHz. Frequency response for band 4 (5.4-18 GHz) is ±3.5 dB and ±5.0 dB for band 5 (15.0-21.0 GHz).

15. Check Display Accuracy and Range

80 dB in 10 dB/DIV mode, with an accuracy of ±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over the 80 dB window; 16 dB in 2 dB/DIV mode with an accuracy of ± 0.4 dB/2 dB to a maximum cumulative error of ±1.0 dB/dB over the 16 dB window; Lin mode is ± 5% of full scale.

a. Test equipment setup is shown in Figure 4-14. Apply a 100 MHz, +10 dBm signal, from the Signal Generator, through external attenuators set to 0 dB, to the RF INPUT.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 20 kHz, Vertical Display to 10 dB/DIV, MIN RF ATTEN at 0 dB, REF LEVEL to +10 dBm, and PEAK/AVERAGE control fully clockwise. Activate AUTO RESOLN and the NARROW Video Filter.

c. Carefully adjust the generator output so the signal level is at the top graticule line.

d. Add 80 dB of external attenuation in 10 dB steps and note that the signal steps down screen in 10 dB (±1.0 dB) steps. Maximum cumulative error should not exceed 2.0 dB over the display window.

e. Return the external attenuation to 0 dB and change the Vertical Display to 2 dB/DIV. Change the RESOLUTION BANDWIDTH to 100 kHz and set the signal peak at the reference (top) graticule line, with the generator output control.

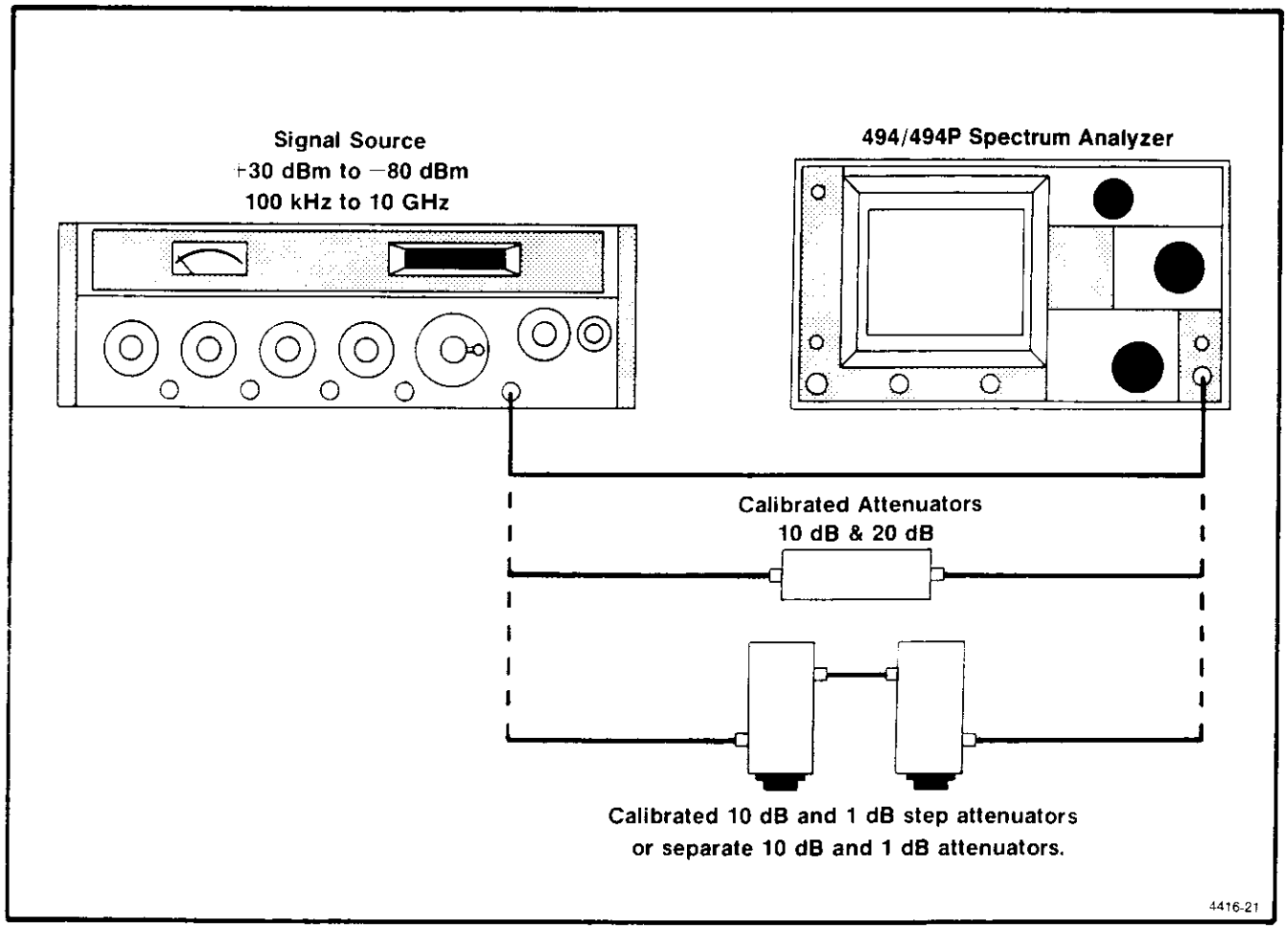


Figure 4-14. Test equipment setup for checking display accuracy, attenuator and gain accuracy, and preselector image rejection.

f. Add 16 dB of external attenuation, in 2 dB steps, and check the display accuracy. Error should not exceed ±0.4 dB/2 dB or exceed a cumulative deviation of ±1.0 dB over the 16 dB window.

g. Return the external attenuation to 0 dB. Change the Vertical Display to LIN. Adjust the signal generator output for a full screen signal display.

h. Add 6 dB of external attenuation. Note that the signal amplitude decreases to within ±0.4 dB of half screen.

i. Add an additional 6 dB of attenuation. Note that the signal amplitude decreases to within ±0.4 divisions of 1/4 screen or half the previous amplitude.

j. Add an additional 6 dB of attenuation. Signal amplitude should decrease to 1.0 ±0.4 divisions.

k. Return the Vertical Display to 10 dB/DIV and disconnect the signal to the RF INPUT.

16. Check Preselector Ultimate Rejection

This is a check of preselector operation, not a performance requirement specification.

a. Test equipment setup is shown in Figure 4-14. Apply a 3.5 GHz, −30 dBm, signal from the Signal Generator to the RF INPUT.

b. Set the FREQUENCY to 3.5 GHz, FREQ SPAN/DIV to 10 kHz, REF LEVEL to −30 dBm, MIN RF ATTEN at 0 dB, TIME/DIV to AUTO, and Vertical Display of 10 dB/DIV. Activate AUTO RESOLN and WIDE Video Filter.

c. Adjust the Signal Generator output for a full screen display. Peak the response with the MANUAL PEAK control or AUTO PEAK mode.

d. Change the FREQ RANGE to band 3 (3.0-7.1 GHz).

e. Check the display for any spurious signals. Any spurii above 70 dB down from the level established in part c, is an indication that the YIG-tuned preselector filter could be defective.

17. Check RF Attenuator Accuracy

Error is within 0.3 dB/10 dB to a maximum of 0.7 dB, over the 60 dB range, to 4 GHz; and within 0.5 dB/10 dB to a maximum of 1.4 dB, over the 60 dB range, to 21 GHz

NOTE

The RF Attenuator is factory checked to ensure accuracy. Any change in characteristics should be readily noticed in operation. The Operational Check of the controls and selectors, should detect any defect. In this procedure, external 10 dB, 20 dB, or 30 dB step attenuators, calibrated by the user or manufacturer to within 0.05 dB, are used as a standard to check the attenuation steps of the RF attenuator.

a. Test equipment is shown in Figure 4-14. Apply a 0 dBm, 4 GHz signal, from a Signal Generator through 30 dB of calibrated attenuation, to the RF INPUT.

b. Set the FREQUENCY to 4 GHz, FREQ SPAN/DIV to 20 kHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to −30 dBm, and Vertical Display factor to 10 dB/DIV.

c. Peak the signal response with MANUAL PEAK or AUTO PEAK mode. Activate 1 dB/div, via the Data Entry keyboard, and press NARROW Video Filter. Adjust the Signal Generator output so the top of the signal is on some graticule reference line, such as seven divisions. Activate SAVE A.

d. Change the REFERENCE LEVEL 10 dB by switching to −20 dBm (this will add 10 dB of RF ATTENuation).

e. Remove 10 dB of external attenuation and activate B−SAVE A. Compare the difference between the reference level and the new level. Variation, plus the calibrated 10 dB external attenuator correction factor, must not exceed 0.3 dB. Deactivate SAVE A and B−SAVE A.

f. Readjust the Signal Generator output to establish a new reference level. Repeat the process to check the 20 dB attenuator by switching the REF LEVEL from −30 dBm to −10 dBm, for 20 dB ATTEN, then remove 20 dB of external attenuation. Attenuation error must not exceed 0.6 dB.

g. Reinstall the 30 dB of external attenuation and set the REF LEVEL to −30 dBm. Re-establish a signal reference level as described above.

h. Check the 30 dB attenuator against the external standard, by switching the REF LEVEL to 0 dBm, for 30 dB RF ATTEN, then remove 30 dB of external attenuation. Error must not exceed 0.7 dB. (Include the calibrated attenuator correction factor.)

i. Since the remaining 60 dB range of the RF ATTENuator is obtained by the combination of these three attenuators, this completes the check of the RF attenuator. Error of any combination must not exceed 0.7 dB.

18. Check IF Gain Accuracy ± 0.2 dB/dB and ±0.5 dB/9 dB to a maximum of ±2 dB over the full 97 dB range

NOTE

This check requires calibrated attenuators as the standard to check the 10 dB and 1 dB steps. When making signal measurements within 10 dB of the noise floor, a correction factor should be used to correct for the logarithmic addition of noise in the system and analyzer, as shown in Table 4-4.

a. Equipment setup is shown in Figure 4-14. Apply a 100 MHz, −20 dBm signal, from the Signal Generator, through 10 dB and 1 dB step attenuators (set at 0 dB), to the RF INPUT; or, directly to the RF INPUT of the 494/494P, if individual fixed attenuators are to be used as the standard.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 10 kHz, REF LEVEL to −20 dBm, and MIN RF ATTENUATOR to 0 dB. Activate 1 dB/div and WIDE Video Filter.

c. Adjust the output of the Signal Generator for a signal amplitude of six divisions, with the top of the signal positioned at the 6th graticule line.

d. Activate MIN NOISE and note signal level shift. Shift must not exceed ± 0.8 dB, or 4 minor divisions (attenuator plus gain accuracies).

e. Adjust the output of the Signal Generator to re-position the signal level to the graticule reference line.

f. Switch the REF LEVEL from −10 dBm to −20 dBm in 1 dB steps, adding 1 dB of external attenuation at each step. Note incremental accuracy and the 10 dB gain accuracy. Incremental accuracy must be within 0.2 dB/dB (0.5 minor division). Maximum cumulative error must not exceed 0.5 dB (1.5 minor divisions) except when stepping from the 9 dB to 10 dB increment, where the error could be an additional 0.5 dB. This exception does not apply when stepping from −69 to −70 dBm, −79 to −80, etc.

g. Deactivate MIN NOISE. Return the 1 dB step attenuator to 0 dB, decrease the Signal Generator output to 10 dB or add 10 dB of external attenuation. Readjust the generator output so the signal level is again at the reference line (6 division amplitude).

h. Change the REF LEVEL from −20 dBm to −30 dBm, in 1 dB increments, with the 1 dB step attenuator, and note incremental and 10 dB step accuracies.

i. Return the 1 dB step attenuator to 0 dB. Decrease the signal level 10 dB, with external attenuation, or with the Signal Generator output level control, then re-establish the signal reference amplitude.

j. Check the −30 dBm to −40 dBm gain accuracies using the above procedure.

k. Repeat the procedure checking gain accuracies to −60 dBm.

l. Establish a signal reference amplitude of −60 dBm, activate NARROW Video Filter, then check gain accuracy to −70 dBm.

m. Decrease the RESOLUTION BANDWIDTH and FREQ SPAN/DIV to 1 kHz. Re-establish a signal reference level of −70 dBm as described previously.

n. Check the −70 dBm to −80 dBm gain accuracies by repeating the process previously described;

o. Decrease the RESOLUTION BANDWIDTH and FREQ SPAN/DIV to 100 Hz or 50 Hz, reestablish the signal reference level and check the −80 dBm to −90 dBm and −90 to −100 dBm gain accuracies. These ranges are directly related to the −60 to −70 dBm check (parts e-o).

19. Check Gain Variation Between Resolution Bandwidths

Variation is less than 0.4 dB with respect to the 1 MHz filter and less than 0.8 dB between any two filters. Before

Table 4-4
CORRECTION FACTOR TO DETERMINE TRUE SIGNAL LEVEL

Ratio in dB of signal plus noise	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	12.0	14.0
Subtract this correction factor for true signal level	3.0	2.20	1.65	1.26	0.97	0.75	0.58	0.46	0.28	0.18

performing this check, do a front panel CAL procedure (press <SHIFT> CAL and perform the steps called out).

a. Apply the Calibrator signal to the RF INPUT, set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, RESOLUTION BANDWIDTH to 1 MHz, REF LEVEL to −18 dBm, TIME/DIV at AUTO, and Vertical Display to 2 dB/DIV. Activate the MIN NOISE so RF ATTEN is 0 dB.

b. Change the Vertical Display to 1 dB/DIV by pressing <SHIFT> dB/DIV, and enter 1 dB/DIV via the Data Entry keyboard. Press FINE to activate the delta A mode.

c. Adjust the REFERENCE LEVEL for a signal amplitude of six divisions, then change the RESOLUTION BANDWIDTH to 100 kHz and FREQ SPAN/DIV to 10 kHz.

d. Check — The signal amplitude deviation from the 1 MHz reference should not change more than 0.4 dB.

e. Change the RESOLUTION BANDWIDTH to 10 kHz and the FREQ SPAN/DIV to 1 kHz.

f. Check — The signal amplitude should not change more than 0.8 dB from the amplitude at 100 kHz resolution and no more than 0.4 dB from the 1 MHz reference level.

g. Repeat the procedure to check the remaining filters (1 kHz, 100 Hz, and 30 Hz) to verify that the signal amplitude does not change more than 0.4 dB from the 1 MHz filter level or a total of 0.8 dB from any filter.

20. Sensitivity (refer to Table 4-5)

NOTE

Sensitivity is specified according to the input mixer average noise level. The Calibrator signal is the reference used to calibrate the display.

a. Remove the Calibrator signal from the RF INPUT. Set the Vertical Display to 10 dB/DIV, REF LEVEL to −30 dBm, FREQ SPAN/DIV to 5 MHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV at 1 s, and FREQ RANGE 0 - 1.8 GHz. Turn the PEAK/AVERAGE control fully clockwise so the cursor is at the top of the screen and activate the WIDE Video Filter.

b. Check— The noise floor (level) should be −80 dBm or less (as indicated in Table 4-5) or 50 dB down from the −30 dBm REF LEVEL.

c. Change the REF LEVEL to −40 dBm, FREQ SPAN/DIV to 1 MHz, and RESOLUTION BANDWIDTH to 100 KHz.

d. Check — The average noise level should be −90 dBm or less or 50 dB below the REF LEVEL.

e. Change REF LEVEL to −60 dBm, FREQ SPAN/DIV to 10 kHz, TIME/DIV to AUTO, RESOLUTION BANDWIDTH to 1 kHz, and activate the NARROW Video Filter.

f. Check — The average noise level for the 1 kHz resolution bandwith should be below the level listed in Table 4-5.

g. Change REF LEVEL to −70 dBm, FREQ SPAN/DIV to 200 Hz, and RESOLUTION BANDWIDTH BANDWIDTH to 100 HZ.

h. Check — The noise level for the 100 Hz resolution bandwidth is no more than that listed in Table 4-5.

i. Change RESOLUTION BANDWIDTH to 30 Hz and FREQ SPAN/DIV to 50 Hz.

j. Check — The noise level for the 30 Hz resolution bandwidth is as listed in Table 4-5.

k. Repeat this procedure for the remaining coaxial input frequency range (0 to 21 GHz). If desired, the sensitivity for the waveguide bands can be checked as per the listings in Table 4-5. The Figures for the 50 GHz to 140 GHz range are typical and not intended as a performance requirement.

21. Check Spurious (Residual) Response

With no input signal, residual spurii are −100 dBm or less, with reference to the mixer input and fundamental mixing for bands 1-3.

a. Remove any signal connected to the RF INPUT. Set the FREQ SPAN/DIV to 10 MHz, RESOLUTION BANDWIDTH to 10 kHz, REF LEVEL to −50 dBm, TIME/DIV at AUTO, and activate 10 dB/DIV.

b. Scan the frequency range of bands 1, 2, or 3 in 100 MHz increments. Note the amplitude of any spurious response. Spurii amplitude must not exceed −100 dBm. (If delta F is activated after each increment, it easier to determine 100 MHz increments.)

22. Intermodulation Distortion

Third order products, within any frequency span, from 50 kHz to 18 GHz, are 70 dB down from any two on-screen signals; and from 1.7 to 1.8 GHz within any frequency span, IM from any two −40 dBm signals, is at least −70 dBc.

a. Equipment setup is shown in Figure 4-15. Set the FREQ SPAN/DIV to 5 MHz, RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to −30 dBm, and FREQUENCY

Table 4-5
494/494P SENSITIVITY

This table shows the equivalent maximum input noise (average noise for each resolution bandwidth with internal mixer and TEKTRONIX High Performance Waveguide Mixers.

Band/Frequency	Equivalent Input Noise (dBm) versus Resolution Bandwidth					
	1 MHz	100 MHz	10 kHz	1 kHz	100 Hz	30 Hz
Band 1-3 50 kHz-7.1 GHz	−80	−90	−100	−110	−118	−121
Band 4 5.4-12.0 GHz	−65	−75	−85	−95	−103	−106
Band 5 15.0-21.0 GHz	−55	−65	−75	−85	−93	−96
[a]Band 6 18.0-26.5 GHz	−70	−80	−90	−100	-108	−111
[a]Band 7 26.5-40.0 GHz	−65	−75	−85	−95	−103	−106
[a]Band 8 33-60 GHz	−65	−75	−85	−95	−103	−106
[a]Band 9 50-90 GHz	Typically −95 dBm for 1 kHz resolution bandwidth at 50 GHz, degrading to −85 dBm at 90 GHz.					
[a]Band 10 75-140 GHz	Typically −90 dBm for 1 kHz bandwidth at 75 GHz, degrading to −75 dBm at 140 GHz.					
[a]Band 11 110-220 GHz	Typically −80 dBm for 1 kHz bandwidth at 110 GHz, degrading to −65 dBm at 220 GHz.					
[a]Band 12 170-325 GHz	Typically −70 dBm for 1 kHz bandwidth at 170 GHz, degrading to −55 dBm at 325 GHz.					

[a]TEKTRONIX High Performance Waveguide Mixers

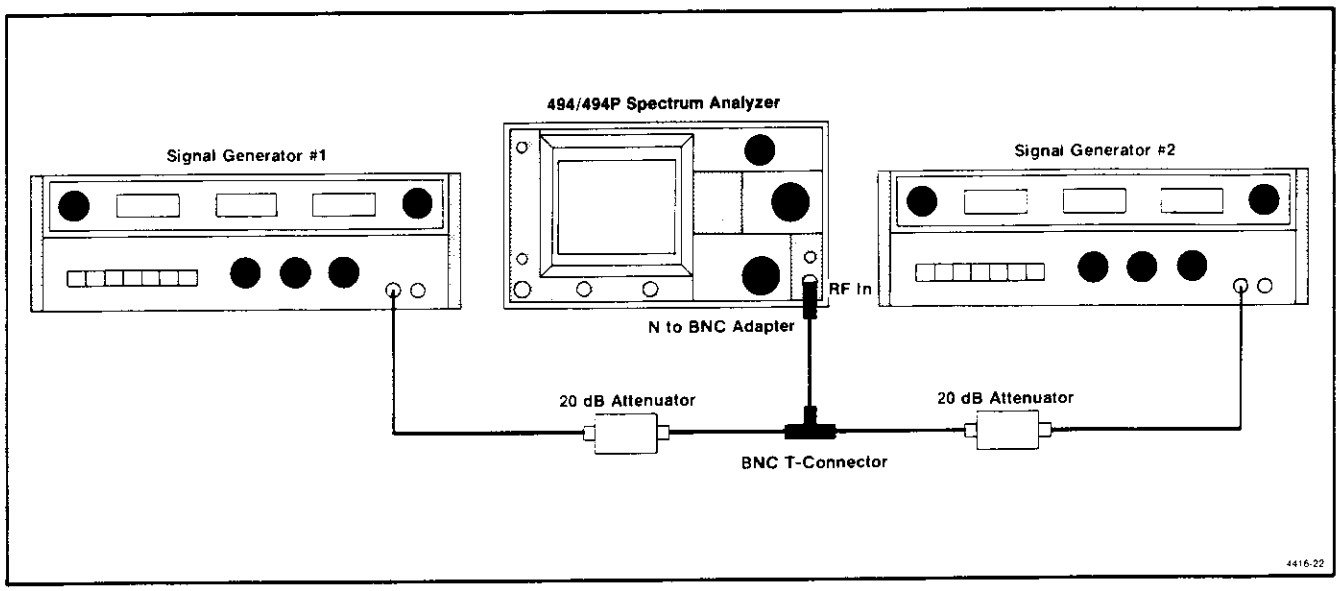


Figure 4-15. Test equipment setup for checking intermodulation distortion.

RANGE to Band 1. Activate 10 dB/DIV, and switch MIN NOISE off.

b. Apply two signals, from two 50 Ω sources, that are separated about 2 MHz and within the frequency range of band 1. Apply the signals through 20 dB attenuators (for isolation), a bnc "T" connector, and bnc-to-n adapter, to the RF INPUT (see Figure 4-15).

c. Adjust the output of the Signal Generators for full screen signals (−10 dBm). Decrease the frequency separation of the signals to 1 MHz and the FREQ SPAN/DIV to 500 kHz. Set the RESOLUTION BANDWIDTH to 10 kHz.

d. Check — that third order intermodulation products (see Figure 4-16) are 70 dB or more down from the input signal level.

NOTE

Use the Video Filter and very slow sweep rates to help resolve these sidebands.

e. Decrease the signal separation and FREQ SPAN/DIV settings and re-check for sidebands. Check for IM products at other spans of the frequency range. IM products should be −70 dBc or more.

f. Change the FREQUENCY RANGE to 1.7 - 5.5 GHz (band 2), FREQ SPAN/DIV to 50 MHz, and RESOLUTION BANDWIDTH to 100 kHz.

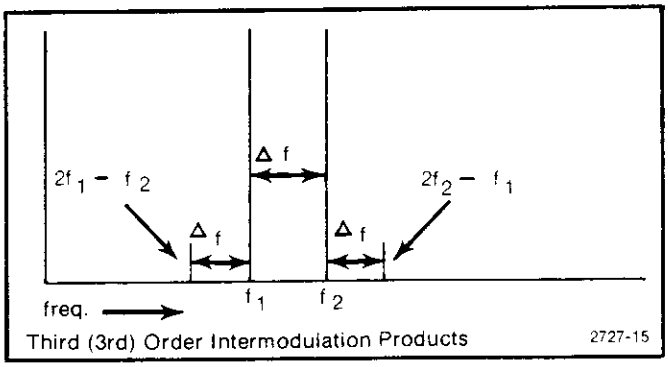


Figure 4-16. Intermodulation products.

g. Apply two full screen (−30 dBm) signals that are above 1.8 GHz to the RF INPUT. Reduce the FREQ SPAN/DIV and RESOLUTION BANDWIDTH so the noise floor is at least 70 dB down from the reference level.

h. Check — to ensure IM products are at least 70 dB down from the input signal level or top of the screen.

i. Change the frequencies of the Signal Generators to frequencies within the 1.7-1.8 GHz range and set the input signal level to −40 dBm by increasing the output of the Signal Generators.

j. Check — that IM products are at least −70 dBc.

23. Check Harmonic Distortion

−60 dBc, 50 kHz - 1.8 GHz; and −100 dBc, 1.7 - 21 GHz; below the level of a full screen signal in MIN DISTORTION mode.

a. Equipment set up is shown in Figure 4-17. Set the FREQ SPAN/DIV to 5 MHz, REF LEVEL to −30 dBm, and RF ATTEN to 0 dB. Activate AUTO RESOLN, 10 dB/DIV, WIDE Video Filter, MIN DISTORTION, and VIEW A, VIEW B.

NOTE

The frequency used must have harmonics between 1.7 – 21 GHz and the signal generator must have low enough FM to produce a signal to measure 100 dB down.

b. Apply the output of a Signal Generator, through a low-pass or band-pass filter (with a minimum of 40 dB rolloff, to attenuate multiples of the generator frequency) to the RF INPUT. (Frequency of the Signal Generator depends on the frequency characteristics of the filter.)

c. Set the 494/494P FREQUENCY to that of the applied signal frequency and adjust the generator output for a full screen (−30 dBm) signal.

d. Press Δ F and adjust the CENTER FREQUENCY to the 2nd multiple of the input frequency. Set the REF LEVEL to −50 dBm, the FREQ SPAN/DIV to 500 kHz, and the RESOLUTION BANDWIDTH to 10 kHz.

e. Check — the display for harmonic response of the input signal. Harmonic spurii must be down at least 40 dB from the top of the screen or 60 dB below the −30 dBm carrier.

f. Set the CENTER FREQUENCY to the 3rd harmonic.

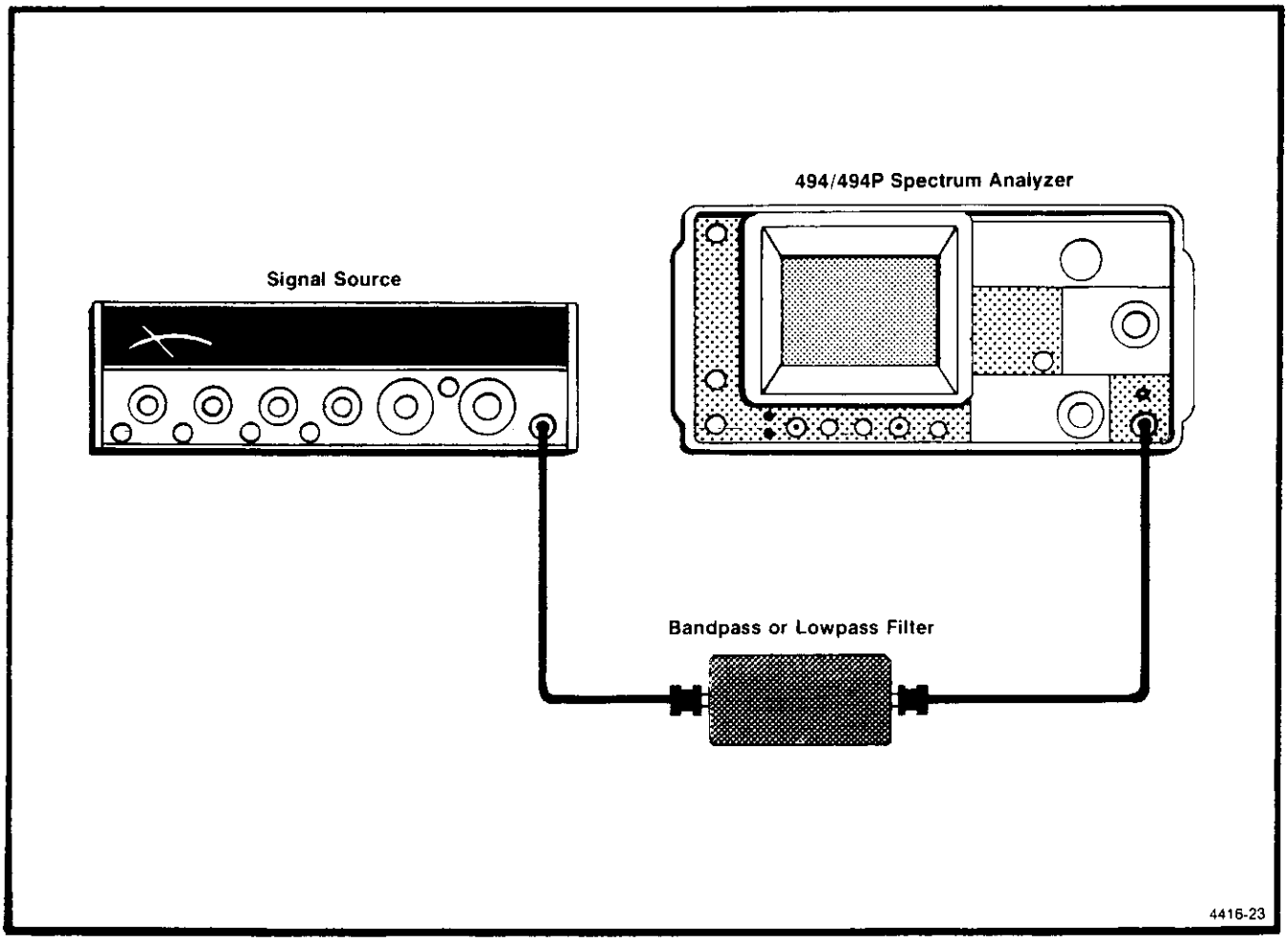


Figure 4-17. Equipment setup for checking harmonic distortion.

g. Check — for harmonic spurii. Again, responses must be at least 40 dB down from the top of the screen or −60 dBc from the fundamental.

h. Set the REF LEVEL to −70 dBm, the FREQ SPAN/DIV to 2 kHz, and the RESOLUTION BANDWIDTH to 100 Hz. Deactivate the WIDE Video Filter.

i. Check — that harmonic spurii are at least 60 dB down from the top of the screen (−100 dBc).

24. Check LO Emission Out the RF Input

Emission is no more than −70 dBm.

a. Connect a sensitive power meter to the RF INPUT so emissions can be measured directly, or connect a high frequency Spectrum Analyzer, set to observe the 2 GHz to 6 GHz range, to the RF INPUT.

b. Set the TIME/DIV to MNL.

c. Check — for any indication of LO emission. Any emission must be less than −70 dBm.

25. Check 1 dB Compression Point

1 dB compression, 1.7 - 2.0 GHz, is −28 dBm or more, otherwise −18 dBm.

a. Equipment setup is shown in Figure 4-18.

b. Connect the power meter with its sensor to the Calibrated Output of the Signal Generator. Set the generator to 1.7 GHz and adjust the output for 0 dBm, as indicated on the power meter.

NOTE

Calibrate the power meter before making this measurement.

c. Disconnect the power meter from the Signal Generator and connect the generator output through 1 dB and 10 dB step attenuators to the RF INPUT of the 494/494P. Set the attenuators for 20 dB of attenuation (10 dB per attenuator).

d. Connect the 10 MHz IF output (on the rear panel of the 494/494P) through a 1 dB step attenuator, to the RF

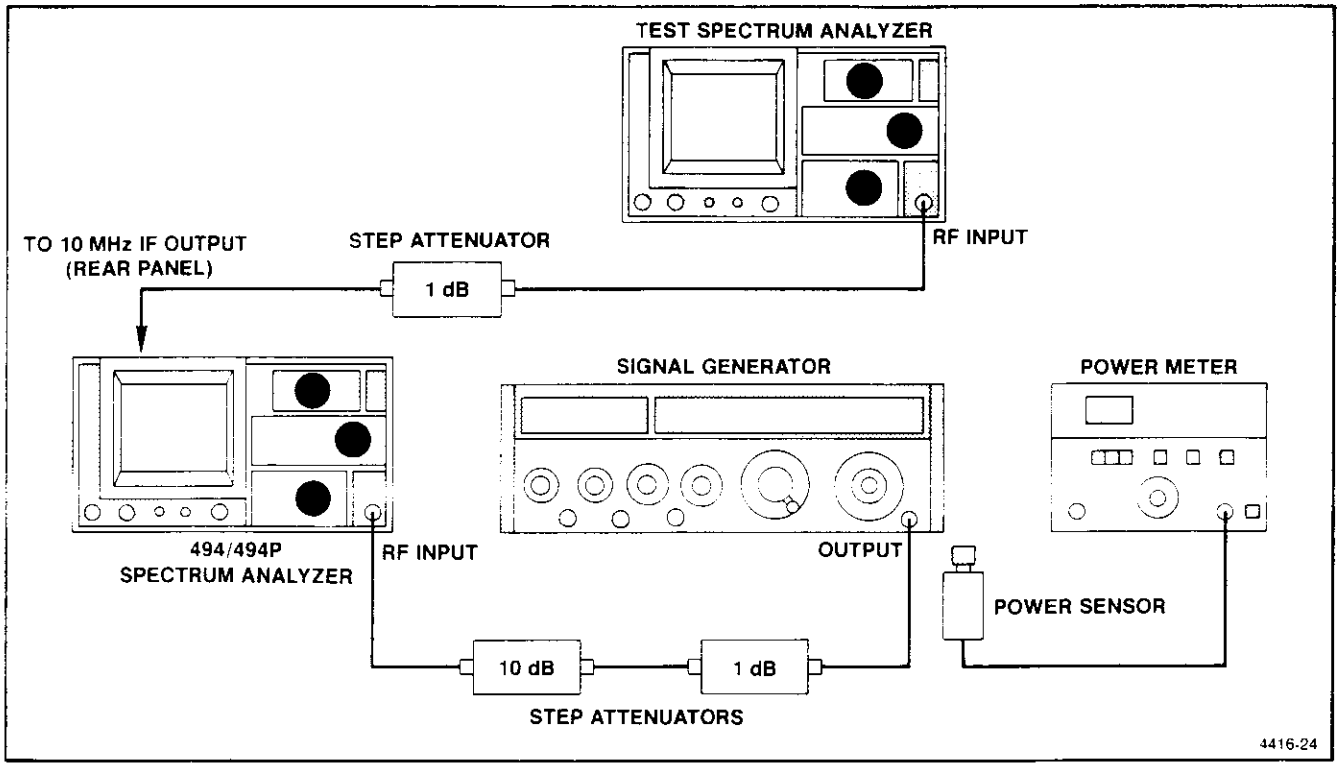


Figure 4-18. Test equipment setup for checking 1 dB input compression point.

Input of a test Spectrum Analyzer. Set the step attenuator for 0 dB attenuation.

e. Set the test Spectrum Analyzer Frequency to 10 MHz, Frequency Span/Div to 100 MHz, Ref Level to −20 dBm, Time/Div to Auto, and activate 2 dB/Div and Auto Resoln.

f. Set the 494/494P FREQUENCY to 1.7 GHz, FREQ SPAN/DIV to 100 kHz, REF LEVEL to −30 dBm, TIME/DIV to AUTO, and activate 10 dB/DIV and AUTO RESOLN.

g. On the 494/494P, activate ZERO SPAN and adjust the CENTER FREQUENCY control to maximize the 10 MHz signal on the test Spectrum Analyzer display.

h. Adjust the test Spectrum Analyzer Ref Level for a four division signal amplitude.

i. Increase the input signal level, to the 494/494P, 1 dB by switching out 1 dB of attenuation between the Signal Generator and the input to the 494/494P. Add 1 dB of attenuation between the 10 MHz output and the test Spectrum Analyzer.

j. Check — the 10 MHz signal amplitude on the test Spectrum Analyzer display should remain the same.

k. Continue to increase the input signal level to the 494/494P by 1 dB increments while increasing the attenuation between the 10 MHz out and the test Spectrum Analyzer until the signal amplitude decreases 1 dB (0.5 division).

l. Check — the 1 dB compression point should be −18 dBm or less (18 dB or less attenuation between the generator and the input of the 494/494P).

m. Check Band 2 (1.7 - 2.0 GHz) compression point as follows:

(1) Deactivate ZERO SPAN, switch the FREQUENCY RANGE to Band 2, and set the FREQUENCY to 1.7 GHz (reference Level −30 dBm).

(2) Set the step attenuators, between the Signal Generator and the RF INPUT, to 30 dB (input to the 494/494P is now −30 dBm).

(3) Peak the signal response with MANUAL PEAK or AUTO PEAK.

(4) Set the attenuator, between the 10 MHz IF out and the test Spectrum Analyzer, to 0 dB.

(5) Activate ZERO SPAN and adjust the test Spectrum Analyzer Reference Level for an on screen display. Maximize the response by tuning the 494/494P CENTER FREQUENCY control.

(6) Set the test Spectrum Analyzer response to some reference level (such as 4 divisions) and repeat the above procedure to check the 1 dB compression point at 1.7 GHz.

(7) Compression should not occur until the input signal level is −28 dBm or more (28 dB external attenuation between the Signal Generator and the 494/494P RF INPUT).

(8) Deactivate ZERO SPAN and set the 494 FREQUENCY to 2.0 GHz.

(9) Return the step attenuators to 30 dB and 0 dB. Set the frequency of the Signal Generator to 2.0 GHz and repeat the above procedure to check 1 dB compression point at 2.0 GHz.

(10) 1 dB compression point should not occur unitl the input signal level to the RF INPUT is −28 dBm or more.

26. Check External Reference Input Power

+15 dBm to −15 dBm; 1,2,5, or 10 MHz.

a. Equipment setup is shown in Figure 4-19. Connect the output of the Signal Generator to a Frequency Counter and set the generator frequency to 10 MHz ±50 Hz.

b. Disconnect the counter and apply the generator output to the EXTERNAL REFERENCE Input connector (on the rear panel) of the 494/494P. Set the generator output to +15 dBm.

c. Check — the crt readout for REF OSC IN USE should read "EXT".

d. Connect the 494/494P CAL OUT to the counter and note that the counter readout is 10 times the external reference source.

e. Decrease the Signal Genertor output to −15 dBm and note that the crt readout is still "EXT" and the Frequency Counter still reads 10X the reference signal frequency. If the crt readout changes to: "EXT—UNLK", recheck the external reference source for 10 MHz ±100 Hz at −15 dBm.

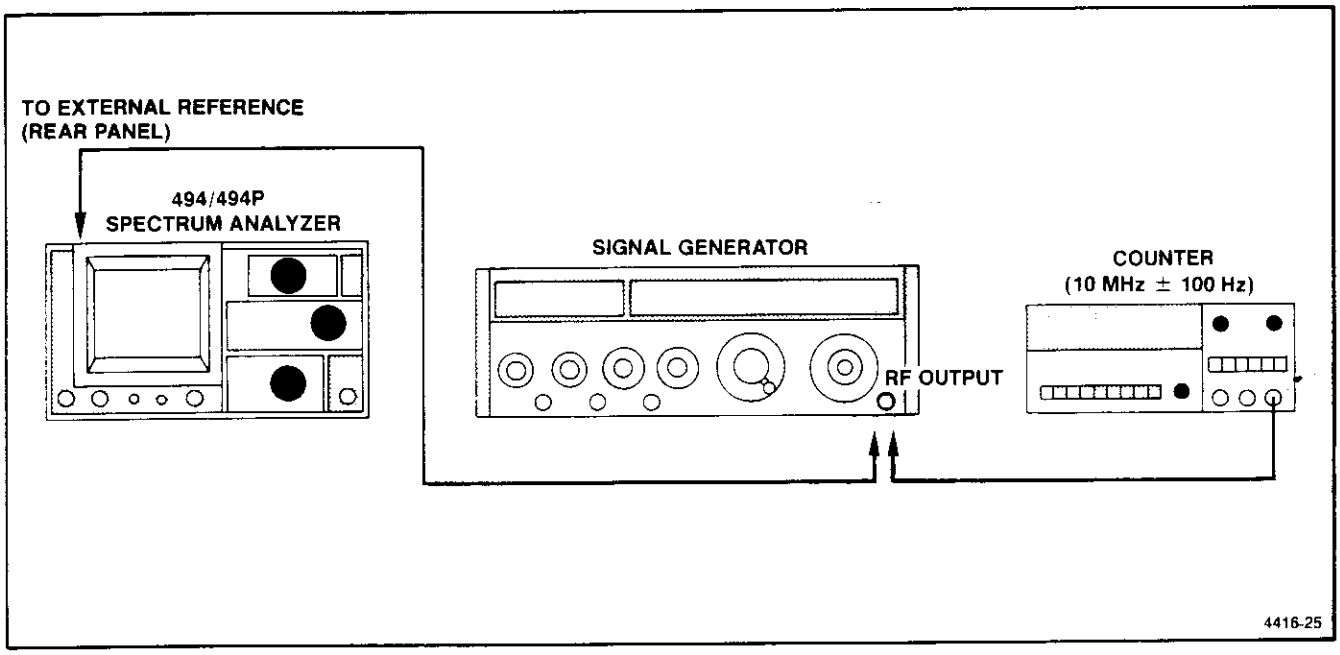


Figure 4-19. Test equipment setup for checking external reference input power.

27. Check Triggering Operation and Sensitivity

Sensitivity, for internal trigger, is 2.0 divisions or more; and 1.0 V peak, 15 Hz to 1 MHz, for external trigger.

a. Equipment setup is shown in Figure 4-20. Apply 100 MHz at −30 dBm from a Signal Generator, that is modulated by the output of a Sine-Wave Generator, to the RF INPUT. Monitor the output of the Sine-Wave Generator with a test Oscilloscope.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 1 MHz, TIME/DIV to 20 ms, and REF LEVEL to −30 dBm. Activate LIN Vertical Display.

c. Decrease the output of the Signal Generator so the display is half screen, then modulate the signal with a 1 kHz sine wave.

d. Activate ZERO SPAN and adjust the CENTER FREQUENCY control if necessary for maximum response.

e. Adjust the Sine Wave Generator output for a modulation amplitude of two divisions, then activate INT Triggering.

f. Check the internal trigger operation through the 15 Hz to 1 MHz frequency range.

NOTE

Because of deflection amplifier response, the display amplitude will decrease at the high frequency end.

The triggering signal can also be applied to the MARKER/VIDEO connector on the back panel if a jumper is connected between pins 1 and 5 (Video Select) of the rear-panel ACCESSORIES connector (Figure 4-21).

g. Disconnect the test equipment. Apply a 1 kHz signal from the Sine Wave Generator, through a bnc "T" connector and coaxial cable, to the HORIZ/TRIG connector (on the back panel of the 494/494P (see Figure 4-22) Monitor the input signal amplitude with a test Oscilloscope.

h. Set the output level of the signal to 2 V peak-to-peak (1.0 V peak) as indicated on the test Oscilloscope (see Figure 4-23).

i. Change the TIME/DIV to 0.2 s. Activate EXT Triggering.

j. Check — that the sweep is triggered over the frequency range of 15 Hz to 1 MHz.

k. Return the Triggering to FREE RUN and the input signal level to 0 V.

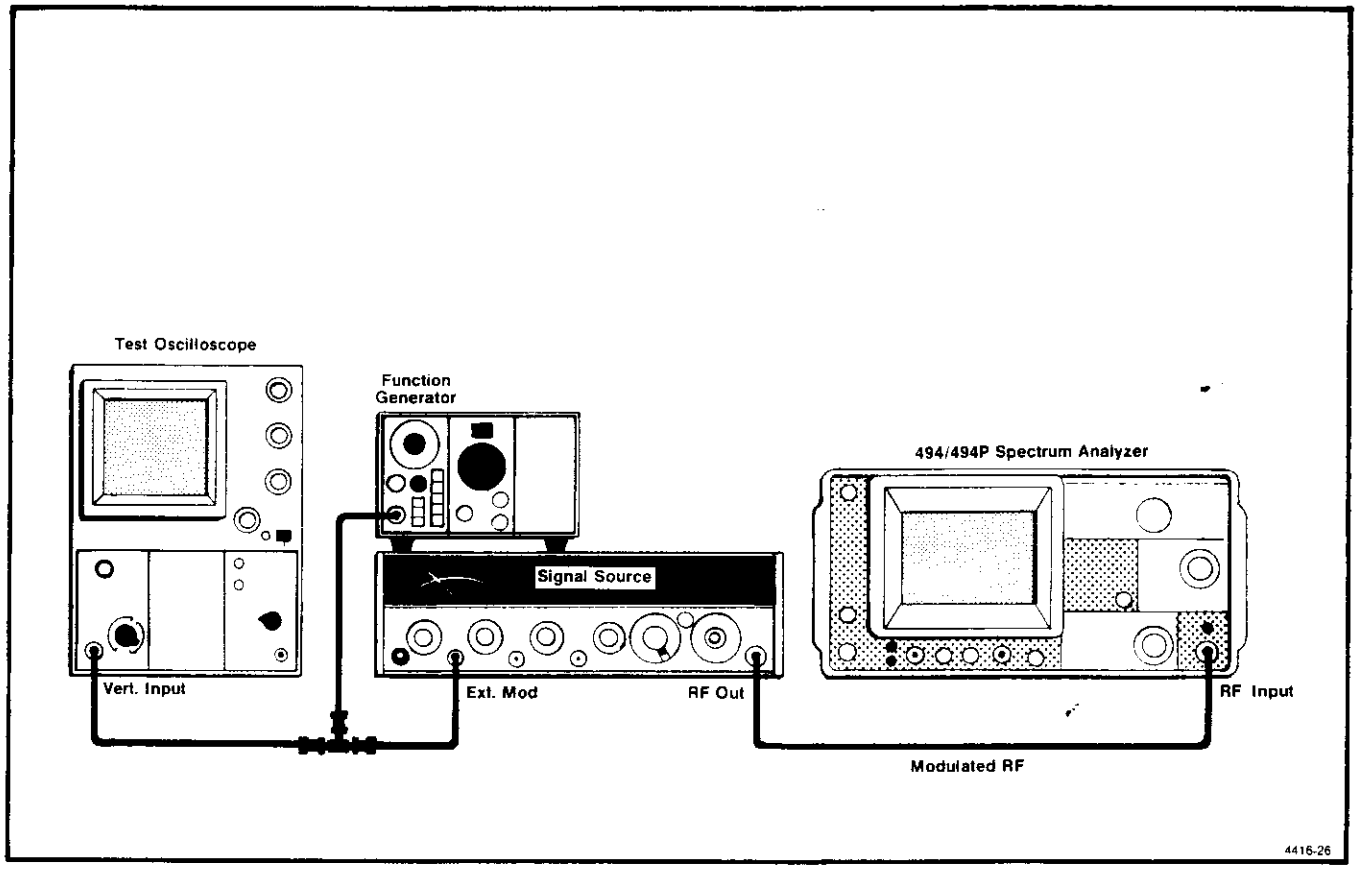


Figure 4-20. Equipment setup for checking internal trigger characteristics.

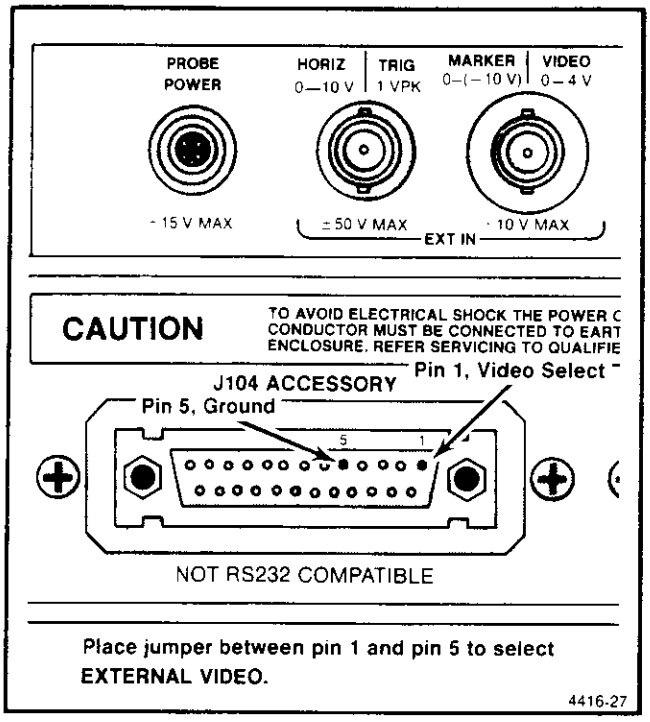


Figure 4-21. External video select pins on ACCESSORIES connector and input to MARKER/VIDEO for signal to check internal triggering.

28. Check External Sweep Operation

0 to 10 V ±1 V should provide a full sweep across the 10 division graticule span. This is an operational check, not a performance requirement.

a. With the test equipment connected as directed for the previous step, set the TIME/DIV to EXT, Vertical Display to 2 dB/DIV, and deactivate VIEW A, VIEW B.

b. With an input signal to the HORIZ/TRIG connector of 0 volt, position the crt beam on the left graticule edge, with the POSITION adjustment. This establishes the 0 V reference.

c. Set the generator frequency to 1 kHz and increase its output for a full 10-division sweep.

d. Check — the peak-to-peak voltage out of the Signal Generator should equal 20 V ±2 V, peak-to-peak, or 10 V ±1 V peak.

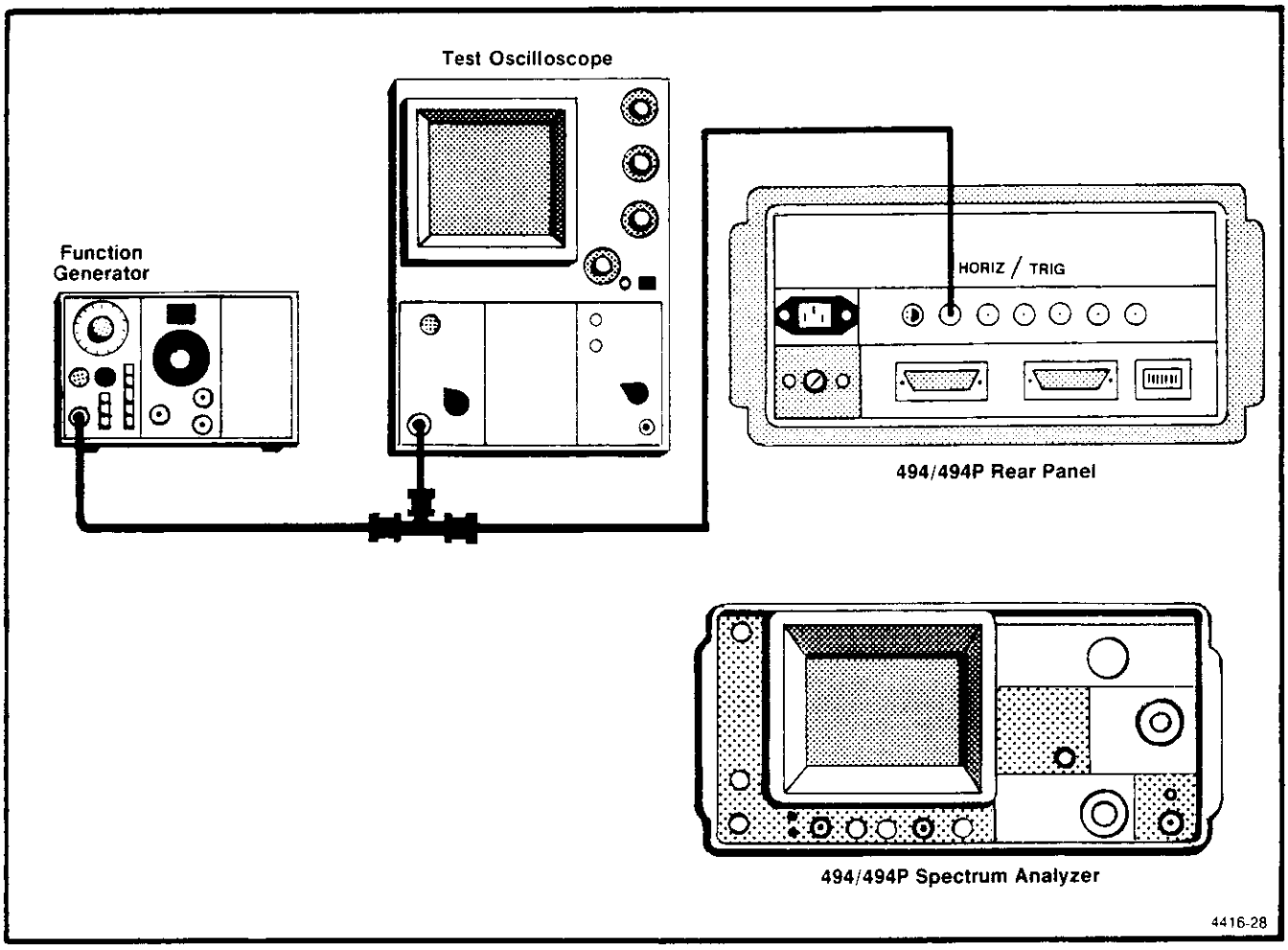


Figure 4-22. Equipment setup for checking external triggering and horizontal input charactertistics.

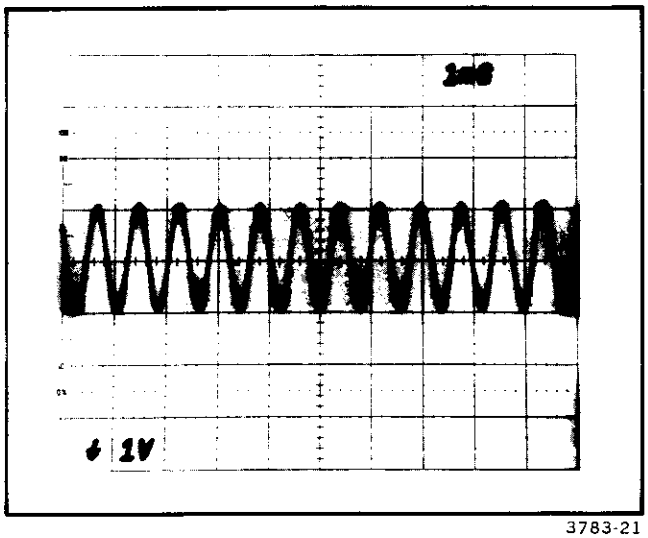


Figure 4-23. Test oscilloscope display of a sinewave input signal to the external TRIG connector (1.0 volt peak at 2.0 V peak-to-peak).

NOTE

A variable voltage source can be used in place of the Sine Wave Generator, to check external sweep operation.

e. Disconnect and remove the test equipment. Return TIME/DIV to AUTO.

29. Check Vertical Output Signal

Output provides 0.5 V ±5% of signal per division of display from the centerline. This is an operational check, not a performance requirement.

a. Connect the VERT OUTPUT to the input of a dc-coupled test Oscilloscope with a sensitivity of 1 V/div and a sweep rate of 10 ms.

b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 100 kHz, TIME/DIV to AUTO, REF LEVEL −20 dBm. Activate 2 dB/DIV and AUTO RESOLN, deactivate VIEW A and VIEW B.

c. Apply the CAL OUT signal to the RF INPUT and verify that the signal amplitude is full screen.

d. Check — the amplitude of the output vertical signal on the test Oscilloscope. Output level should equal, plus and minus 2 V for a total of 4 V ±0.2 V (see Figure 4-24).

30. Check Horizontal Signal Output Level

Output 0.5 V/division, ±5% either side of center screen. This is an operational check, not a performance requirment.

a. Connect a dc-coupled test oscilloscope to the HORIZ OUTPUT connector. Set the TIME/DIV to the MNL position.

b. Adjust MANUAL SCAN control for five division beam deflection from the left to right side of center screen and note the voltage sweep on the test Oscilloscope. The output voltage should vary from −2.5 V to +2.5 V, ±10%.

c. Return the TIME/DIV to AUTO; disconnect and remove the test equipment.

31. GPIB Verification Program (494P only)

This verification program can be used with a TEKTRONIX 4050-Series Computer Terminal to check the functional operation of the GPIB interface in the 494P Spectrum Analyzer. All interface lines are verified as well as all interface messages, except those for parallel poll. In addition, the instrument interface is checked for operation on other primary addresss, as well as the talk-only and listen-only modes.

The program is written in Tektronix 4050 BASIC, and is divided into individual tests, each for a specific interface line, message, or function. The tests start on even 1000 line numbers to allow easy modification of the program.

The following describes the function of each test in the program.

Lines 1-5000: Interfaces to user definable keys for recovery from a failed test.

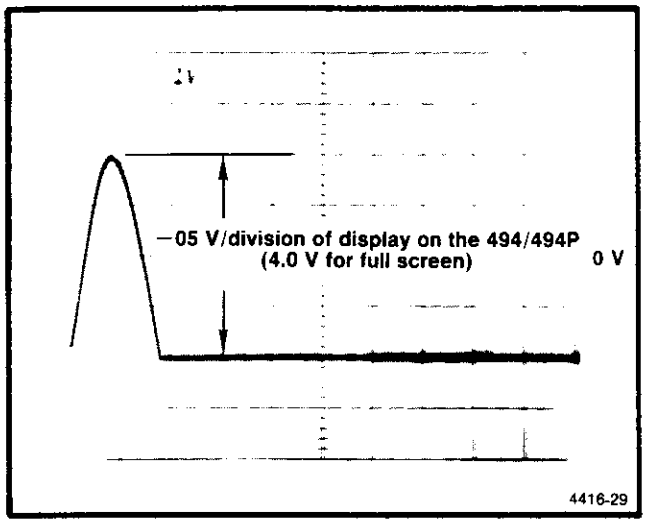


Figure 4-24. Test oscilloscope display of VERTical output with a full screen display on the 494.

Lines 5000-6000: Inputs the primary address of the 494P under test (1 should be used).

Lines 6000-7000: ID query response test. The instrument must be able to talk and listen, to send out its ID? response and manipulate all eight of the DIO lines for the test to be successful.

Lines 7000-8000: Local lock-out test. Tests correct operation of the interface message that should disable all programmable front panel controls.

Lines 8000-9000: Go to LOCAL test. Tests correct operation of the interface message that should enable all front panel controls.

Lines 9000-10000: Group Execute Trigger test. Checks that a GET message does cause the 494P to abort the present sweep and re-arm the trigger, causing a sweep to start and end, sending out an End-of-Sweep SRQ. Thus, the SRQ line, as well as the GET message, is verified.

Lines 10000-11000: Selected Device Clear Test. This test verifies that an SDC message does indeed reset the 494P's GPIB output buffer clearing out it's ID? response.

Lines 11000-12000: Device clear test. This test is identical to the selected device clear test, except the universal command DCL is used instead.

Lines 12000-13000: Addressed as listener, talker test. This test checks to see that the 494P microprocessor correctly recognized that the GPIA chip has been addressed to listen or talk, and sends the appropriate character to the crt readout (L or T).

Lines 13000-14000: Serial Poll test. This checks correct operation of the serial poll enable (SPE) and serial poll disable (SPD) interface messages. The status byte is read, and if anything other than ordinary operation is indicated, the instrument fails the test.

Lines 14000-15000: GPIB rear panel switch test. All five primary address switches are checked for correct operation. Three subroutines are called in the process of testing one address switch. The first two send a formatted messge to the 4050 display, and the third performs the address switch test.

Lines 15000-16000: Line feed or EOI switch test. Checks for correct selection of line feed as a termination when selected by this switch by sending an ID? terminated only by a line feed.

Lines 16000-17000: Talk-only mode test. When selected, this mode should cause the instrument to send a SET? response and (optionally) a CURVE? response whenever the RESET-TO-LOCAL button is pressed. The string received from the instrument is thus examined for existence of a portion of the correct SET? response after the RESET-TO-LOCAL button is pressed.

Lines 17000-18000: Listen-only mode test. When selected, this mode will cause the instrument to respond to any message on the bus, since it is always addressed to listen. The command REF 0 is sent to the bus without addressing the instrument, then the listen-only mode is deselected and the instrument interrogated to see if it did respond to the REF command while in the listen-only mode.

Lines 18000-19000: Interface clean (and Remote Enable) test. This IFC line on the GPIB will unaddress the instrument's interface. This fact is verified by noting that the L is not present in the crt readout, indicating that the IFC line worked; also the REN line will be unasserted when the end statement is executed (except for some early 4052 and 4054's). Thus, a front panel in the local mode is evidence that the REN line was successfully unasserted. (Evidence it was asserted is that the instrument was able to execute commands sent to it by previous tests.)

Lines 19000-end: Utility routines. Rear panel interface switch test text routine puts headers on the interface switch test display. The rear panel test text routine tells the operator what to do after changing the address switches. Test address switch acquires an ID? response from the instrument on its new address during the address switch test. The SRQ handler will handle any 49X SRQ's that occur, although none, except the power-up SRQ, would be expected. (The end of sweep SRQ during the GET test is handled by another SRQ handler.) Delay Generator generates delays for other tests. The Failure Decision Handler allows the program to be restarted with the user definable keys if any test fails.

```
1 GO TO 5000
4 B2=1
5 RETURN
20 B2=5
21 RETURN
5000 REM *** 49XP GPIB VERIFICATION PROGRAM ***
5030 INIT
5040 ON SRQ THEN 19280
5050 DIM V$(400),W$(400)
5060 I7=0
5070 PAGE
5080 PRINT "JJJENTER 49XP'S PRIMARY ADDRESS  (DEFAULT = 1) ";
5090 INPUT T$
5100 IF T$<>"" THEN 5130
5110 A1=1
5120 GO TO 5180
5130 A1=VAL(T$)
5140 IF A1>0 AND A1<31 THEN 5180
5150 PRINT "JJJGERROR!! ";A1;" IS NOT A VALID ADDRESS";
5160 PRINT " ONLY 0 THRU 30 ARE VALID ADDRESSESKK"
5170 GO TO 5080
5180 PAGE
5190 REM
5200 REM
5210 REM
5220 REM
5230 REM
6000 REM ***"ID" QUERY RESPONSE ***
6010 PRINT "*** ""ID"" QUERY RESPONSE ***"
6020 PRINT @A1:"INIT;ID?;SIG"
6030 INPUT @A1:T$
6040 V$=SEG(T$,1,9)
6050 IF V$="ID TEK/49" THEN 6080
6060 PRINT "JJJ*** ""ID"" QUERY RESPONSE *** FAIL ***G"
6070 GO TO 19530
6080 WBYTE @32+A1:64,128,-127
6090 PRINT @A1:"WFM ENC:BIN;CUR?"
6100 PRINT @37,0:37,255,255
6110 INPUT %A1:T$
6120 WBYTE @64+A1:
6130 RBYTE R,R,R,T6
6140 WBYTE @95:
6150 IF R=>128 AND T6<128 THEN 7000
6160 PRINT "JJJ*** DIO8 TEST *** FAIL ***G"
6170 GO TO 19530
6180 REM
6190 REM
6200 REM
6210 REM
6220 REM
7000 REM *** LOCAL LOCK-OUT.............LLO ***
7010 PRINT "*** LOCAL LOCK-OUT.........LLO ***"
7020 WBYTE @32+A1,17:
7030 PRINT @A1:"SET?"
7040 INPUT @A1:V$
```

```
7050 PRINT "II49XP IN LOCAL LOCK-OUT MODE (LLO)"
7060 PRINT "IIATTEMPT TO USE 49XP CONTROLS"
7070 PRINT "IIPRESS RETURN <CR> WHEN DONE ";
7080 INPUT T$
7090 PRINT @A1:"SET?"
7100 INPUT @A1:W$
7110 IF W$<>V$ THEN 7130
7120 GO TO 8000
7130 PRINT "J*** LOCAL LOCK-OUT.............LLO *** FAIL ***G"
7140 GO TO 19530
7150 REM
7160 REM
7170 REM
7180 REM
7190 REM
8000 REM *** GO TO LOCAL.............GTL ***
8010 PRINT @A1:"INIT;TIM?"
8020 INPUT @A1:R
8030 PRINT @A1:"TIM INC"
8040 PRINT "*** GO TO LOCAL.............GTL ***"
8050 WBYTE @32+A1,1:
8060 PRINT @A1:"TIM?"
8070 INPUT @A1:T6
8080 IF R<>T6 THEN 8100
8090 GO TO 9000
8100 PRINT "J**** GO TO LOCAL...........GTL *** FAIL ***G"
8110 GO TO 19530
8120 REM
8130 REM
8140 REM
8150 REM
8160 REM
9000 REM *** GROUP EXECUTE TRIGGER........GET ***
9010 PRINT "*** GROUP EXECUTE TRIGGER...GET ***"
9020 ON SRQ THEN 9120
9030 I7=0
9040 PRINT @A1:"INIT;TIM 100M;SIG;EOS ON"
9050 WBYTE @32+A1,8:
9060 T6=3
9070 GOSUB 19390
9080 PRINT @A1:"EOS OFF"
9090 IF I7<>1 THEN 9150
9100 ON SRQ THEN 19280
9110 GO TO 10000
9120 WBYTE @20:
9130 I7=1
9140 RETURN
9150 PRINT "GROUP EXECUTE TRIGGER...GET *** FAIL ***G"
9160 GO TO 19530
9170 REM
9180 REM
9190 REM
9200 REM
9210 REM
10000 REM *** SELECTED DEVICE CLEAR...SDC ***
```

```
10010 PRINT "*** SELECTED DEVICE CLEAR...SDC ***"
10020 PRINT @A1:"ID?"
10030 WBYTE @32+A1,4:
10040 WBYTE @64+A1:
10050 RBYTE R
10060 IF ABS(R)<>255 THEN 10080
10070 GO TO 11000
10080 PRINT "*** SELECTED DEVICE CLEAR.....SDC *** FAIL ***G"
10090 GO TO 19530
10100 REM
10110 REM
10120 REM
10130 REM
10140 REM
11000 REM *** DEVICE CLEAR.....DCL ***
11010 PRINT "*** DEVICE CLEAR.....DCL ***"
11020 PRINT @A1:"ID?"
11030 WBYTE @20:
11040 WBYTE @64+A1:
11050 RBYTE R
11060 IF ABS(R)<>255 THEN 11080
11070 GO TO 12000
11080 PRINT "*** DEVICE CLEAR.....DCL *** FAIL ***G"
11090 GO TO 19530
11100 REM
11110 REM
11120 REM
11130 REM
11140 REM
12000 REM ** ADDRESSED AS LISTENER, TALKER ***
12010 PRINT "*** 49XP ADDRESSED AS LISTENER..***"
12020 WBYTE @32+A1:76,79,82,68,79,-63
12030 T6=1
12040 GOSUB 19390
12050 INPUT @A1:V$
12060 T$=SEG(V$,16,1)
12070 IF T$="L" THEN 12100
12080 PRINT "J*** 49XP ADDRESSED AS LISTENER *** FAIL ***G"
12090 GO TO 19530
12100 PRINT "*** 49XP ADDRESSED AS TALKER.... ***"
12110 PRINT @A1:"INIT;TIM 50M;SIG;SIG;WAI;LORDO?"
12120 INPUT @A1:V$
12130 T$=SEG(V$,16,1)
12140 IF T$="T" THEN 13000
12150 PRINT "*** 49XP ADDRESSED AS TALKER *** FAIL ***"
12160 GO TO 19530
12170 REM
12180 REM
12190 REM
12200 REM
12210 REM
13000 REM *** SERIAL POLL ***
13010 PRINT "*** SERIAL POLL.....SPD/SPE ***"
13020 WBYTE @95,63,24,64+A1:
13030 RBYTE R
```

```
13040 WBYTE @95,25:
13050 IF R=0 OR R=16 THEN 13080
13060 PRINT "J*** SERIAL POLL *** FAIL ***G"
13070 GO TO 19530
13080 T6=3
13090 GOSUB 19390
13100 REM
13110 REM
13120 REM
13130 REM
13140 REM
14000 REM *** GPIB INTERFACE REAR PANEL SWITCH TEST ***
14010 PAGE
14020 A1=2
14030 GOSUB 19000
14040 PRINT " 0 I0 I0 I00010"
14050 GOSUB 19070
14060 GOSUB 19190
14070 PAGE
14080 A1=4
14090 GOSUB 19000
14100 PRINT " 0 I0 I0 I00100"
14110 GOSUB 19070
14120 GOSUB 19190
14130 PAGE
14140 A1=8
14150 GOSUB 19000
14160 PRINT " 0 I0 I0 I01000"
14170 GOSUB 19070
14180 GOSUB 19190
14190 PAGE
14200 A1=16
14210 GOSUB 19000
14220 PRINT " 0 I0 I0 I10000"
14230 GOSUB 19070
14240 GOSUB 19190
14250 REM
14260 REM
14270 REM
14280 REM
14290 REM
15000 REM *** "LF" OR "EOI" SWITCH ***
15010 PAGE
15020 A1=1
15030 GOSUB 19000
15040 PRINT " 0 I0 I 1 I00001"
15050 GOSUB 19070
15060 PRINT "JJTESTING" "LF" "OR" "EOI" "SWITCH"
15070 GOSUB 19190
15080 WBYTE @32+A1:73,68,63,10
15090 INPUT @A1:T$
15100 T$=SEG(T$,1,9)
15110 IF T$="ID TEK/49" THEN 15140
15120 PRINT "J""LF" "OR" "EOI" "SWITCH *** FAIL ***G"
15130 GO TO 19530
```

```
15140 T6=2
15150 GOSUB 19390
15160 REM
15170 REM
15180 REM
15190 REM
15200 REM
16000 REM *** TALK ONLY MODE ***
16010 PAGE
16020 GOSUB 19000
16030 PRINT " 0 I 1 I0 I00001"
16040 GOSUB 19070
16050 PRINT "JJJTESTING TALK ONLY"
16060 INPUT @A1:V$
16070 I7=POS(V$,"FINE OFF",1)
16080 IF I7<>0 THEN 17000
16090 PRINT "JJJTALK ONLY MODE *** FAIL ***G"
16100 GO TO 19530
16110 REM
16120 REM
16130 REM
16140 REM
16150 REM
17000 REM *** LISTEN ONLY MODE ***
17010 PAGE
17020 GOSUB 19000
17030 PRINT " 1 I 0 I 0 I00001"
17040 GOSUB 19070
17050 PRINT "JJJTESTING LISTEN ONLY"
17060 PRINT @A1:"INI"
17070 T6=0.5
17080 GOSUB 19390
17090 WBYTE 82,69,70,32,-48
17100 PAGE
17110 GOSUB 19000
17120 PRINT " 0 I 0 I 0 I00001"
17130 GOSUB 19070
17140 PRINT @A1:"REF?"
17150 INPUT @A1:V$
17160 IF V$<>"REFLVL +0.0" THEN 17180
17170 GO TO 18000
17180 PRINT "JJJLISTEN ONLY MODE *** FAIL ***G"
17190 GO TO 19530
17200 REM
17210 REM
17220 REM
17230 REM
17240 REM
18000 REM *** INTERFACE CLEAR AND REMOTE ENABLE TEST.....IFC & REN ***
18010 PAGE
18020 PRINT "JJJTESTING IFC(INTERFACE CLEAR), AND REN(REMOTE ENABLE)"
18030 WBYTE @32+A1:
18040 T6=3
18050 GOSUB 19390
18060 PRINT "JJCHECK THE 49XP CRT, FOR AN" "L" "BETWEEN THE VERTICAL"
```

```
18070 PRINT "DISPLAY AND THE MIN RF ATTEN READOUTS."
18080 PRINT "JPRESS RETURN TO CONTINUE.";
18090 INPUT P$
18100 INIT
18110 PRINT "JIF AN" "L" "IS STILL PRESENT, THE IFC LINE IS FAULTY,"
18120 PRINT "IF THE" "L" "VANISHED, IFC TESTED OK."
18130 PRINT "JJCHECK ALSO THE 49XP FRONT PANEL FOR PROPER LOCAL CONTROL"
18140 PRI "IF THE FRONT PANEL IS LOCKED OUT, THE REN LINE IS FAULTY, IF"
18150 PRINT "NOT, REN TESTED OK"
18160 PRINT "JJJGPIB VERIFICATION COMPLETEG"
18170 END
18180 REM
18190 REM
18200 REM
19000 REM *** REAR PANEL INTERFACE SWITCH TEST TEXT ROUTINE ***
19010 PRINT "SET GPIB ADDRESS SWITCHES TO:"
19020 PRINT "JJLISTENITALKILF ORI ADDRESS"
19030 PRINT " ONLYIONLYIEOIII16 8 4 2 1"
19040 PRINT "------I----I-----I----------"
19050 RETURN
19060 REM
19070 REM *** REAR PANEL TEST TEXT ROUTINE ***
19080 PRINT "JJAFTER CHANGING THE SWITCHES, ";
19090 PRINT "PRESS THE REMOTE/LOCAL BUTTON ONCEJJ"
19100 PRINT "I(NOTE: IF YOU GET A GPIB INTERFACE ERROR MESSAGE,"
19110 PRINT "I       IT MEANS THAT THE SWITCH(ES) WEREN"T "
19120 PRINT "I       READ CORRECTLY. TO RE-TEST, TYPE"
19130 PRINT "I       ""RUN"" FOLLOWED BY THE LINE NUMBER IN THE"
19140 PRINT "I       ERROR MESSAGE)"
19150 PRINT "JJIPRESS RETURN <CR> WHEN DONE ";
19160 INPUT T$
19170 RETURN
19180 REM
19190 REM *** TEST ADDRESS SWITCH ***
19200 PRINT @A1:"ID?"
19210 INPUT @A1:T$
19220 T$=SEG(T$,1,8)
19230 IF T$="ID TEK/49" THEN 19260
19240 PRINT "ADDRESS SWITCH TEST FAIL"
19250 GO TO 19530
19260 RETURN
19270 REM
19280 REM *** SRQ HANDLER ***
19290 T6=3
19300 GOSUB 19390
19310 POLL Z1,Z1;A1
19320 PRINT @A1:"ERR?"
19330 INPUT @A1:S$
19340 PRINT "GGAN INTERRUPT OCCURRED ON THE BUS, THE 49XP RETURNS ";S$
19350 PRINT "JPRESS RETURN <CR> TO CONTINUE ";
19360 INPUT T$
19370 RETURN
19380 REM
19390 REM *** DELAY GENERATOR ***
19410 REM *** T6 GIVEN IN SEC (GLOBAL) *** I9 SCRATCH ***
```

```
19420 IF T6<0 THEN 19510
19430 IF RND(0)>0.5 THEN 19490
19440 REM *** 4051 ***
19450 T6=T6*220
19460 FOR I9=1 TO T6
19470 NEXT I9
19480 GO TO 19510
19490 REM *** 4052
19500 CALL "WAIT",T6
19510 T6=0
19520 RETURN
19530 REM **** FAILURE DECISION HANDLER ****
19540 PRINT "JJISELECT A UDK:"
19550 PRINT "I  (1) RE-START"
19560 PRINT "I  (5) END"
19570 SET KEY
19580 B2=0
19590 IF B2<>1 AND B2<>5 THEN 19590
19600 IF B2=5 THEN 19630
19610 PAGE
19620 GO TO 6000
19630 END
```

THEORY OF OPERATION

This section of the manual describes the circuitry in the 494/494P Spectrum Analyzer. The section begins with a general or functional description of the major circuit blocks and systems that make up the 494/494P. This is followed by a more detailed description of the circuitry within each block or section, for example; the display section.

The number in the diamond that is adjacent to the section title refers to the corresponding schematic diagram number. Note that these same numbers are included on diagrams to designate the interconnection between circuits, or, in the case of block diagrams, to the more detailed diagram of that block. Schematic diagrams of the circuits are part of Volume 2, section 10.

FUNCTIONAL AND GENERAL DESCRIPTION

What It Does

The 494/494P Spectrum Analyzer accepts an electrical signal as its input and displays the signal's frequency components on a crt. Signals can be applied directly to the RF INPUT or, if the analyzer is equipped for external mixer operation, to an external mixer, which extends the measurement range of the 494/494P.

The display of the frequency components of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can be plotted, if desired, by connecting a chart recorder through rear-panel connectors. If the instrument is programmable, the display can also be transmitted digitally via the IEEE 488 bus to a GPIB plotter.

Manual operation of the 494/494P Spectrum Analyzer is accomplished with front-panel controls and switches. The 494P (programmable version) can also be operated via the IEEE 488 bus using a straightforward language format.

How It Works

A functional block diagram, located at the front of the Diagrams section in Volume 2, shows how the major sections in the instrument relate and the paths of most major signals. Refer to the diagram while reading this general description.

The 494/494P operates as a swept, narrow-band receiver. As it sweeps or spans a range of frequencies, it moves the crt beam horizontally. When a frequency component of an input signal is detected the beam is deflected vertically as a function of input power at that frequency. The center frequency of each span is set by the CENTER FREQUENCY control or FREQUENCY entry via a Data Entry keyboard. The frequency range of each span is set by the FREQ SPAN/DIV control or settings. The power level, represented by the top of the screen, is set by either the REFERENCE LEVEL control or the Data Entry keyboard.

First, Second, and Third Converters

In the 494/494P Spectrum Analyzer, this swept-frequency analysis is achieved by means of a triple-conversion superheterodyne technique. Each of three frequency converters consist of a mixer, a local oscillator, and appropriate filters. Only one frequency is converted in each mixer to pass through band-pass filters to the detector. This frequency can be changed by changing the frequency of the local oscillators in any one of the converters.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) of either 829 MHz or 2072 MHz, depending on which band is in use. The internal mixer converts signals from 10 kHz to 21 GHz, and external mixers may be used for signals in the millimeter wavelengths. When the internal mixer is used, a preselector or low-pass filter is inserted in the signal path to reduce unwanted signals or images and spurious responses from cluttering the display.

One of two second converters is selected automatically for each band so the input frequency range does not overlap the first IF frequency. Each second converter has its own local oscillator (LO), mixer, and filters. Both down-convert the signal to 110 MHz which is sent to the third converter.

The third converter amplifies the 110 MHz IF signal and converts it to the final intermediate frequency of 10 MHz. The third converter passes the signal to the main IF section for processing and detection.

IF Section

In this section the signal is processed for frequency resolution.Three functions are performed here:

1. Weak signals can be amplified, by switchable amplifiers, so the vertical window (dynamic display range) is shifted up or down. The REFERENCE LEVEL selects the gain and input RF attenuation to frame this window between the top of the display screen or reference level, in dBm or volts, and the bottom of the display.

2. The signal is processed through one of several 10 MHz band-pass filters that can be selected by the RESOLUTION BANDWIDTH control. In the auto mode the microcomputer will select the best combination of bandwidth and sweep time for the selected span, unless overridden by the operator.

3. The signal is amplified by a logarithmic then detected. The output from this detector is a voltage that corresponds to the signal strength, in decibels, which is sent to the vertical channel of the display section to drive the vertical axis of the crt and display the strength of the signal.

Display Section

The display section drives the X,Y, and Z axis of the crt display. Vertical deflection of the beam is increased as the output of the amplitude detector increases. The horizontal position of a signal is controlled by the frequency control section and corresponds to the frequency analyzed at that instant. As the 494/494P spans from low to high frequencies during its analysis, the beam is swept from left to right. When the analyzer tunes through a signal frequency, a vertical deflection shows the strength of the signal.This signal is therefore displayed at a postion on the span that corresponds to its frequency, or, the display is one of amplitude as a function of frequency.

The video amplifier scales the output of the detector for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor filters the video if either the wide or narrow filter is selected.

The display section also drives the crt readout to show control settings. This readout is based on data from the microcomputer which is reading the settings of the front panel controls or data on the GPIB bus.

The sweep is usually fast enough so the display is flicker-free, but at times the sweep must be slowed below the flicker rate. With digital storage the display can be recorded and refreshed at a flicker-free rate.The 494P can read-out the display data, from digital storage, through the IEEE 488 interface.

Frequency Control Section

The 494/494P sweeps through a frequency range that is centered about a frequency set by the frequency control section. The CENTER FREQUENCY control sets the center frequency of either the 1st or 2nd local oscillator.

The output of a sweep generator is scaled by a span attenuator to sweep a range or span of frequencies either side of center. The output of the span attenuator drives the 1st LO for wide spans and the 2nd LO for narrow spans. The output sweep also deflects the crt beam across the horizontal axis as the local oscillators are swept so the display is a spectrum of frequency versus power.

The frequency control section also tunes the preselector so it tracks the signal frequency being detected over the 1.7 to 21 GHz range.

Microwave Counter and Phase Lock Section

The microwave Counter, Harmonic Mixer, and Auxiliary Synthesizer comprise the nucleus of the frequency control hardware. Both the 1st LO and 2nd LO frequencies are controlled via the firmware based control loop. Data from the Counter, is used as feedback to control the oscillator frequency. Accurate signal frequency measurement is also possible by counting the frequency of the 3rd IF.

The Phase Lock system stabilizes the 1st LO frequency to minimize FM'ing or display jitter and increase resolution.

Digital Control Section

Operational modes and internal functions of the 494/494P analyzer are selected and controlled directly from the front panel or remotely controlled from an external controller through a IEEE 488 connector. This connector interfaces to an instrument microcomputer through a General Purpose Interface Bus (GPIB). The modes and functions that are selected are processed and activated by the instrument master microcomputer which talks and listens to all circuits over the instrument bus.

Front panel control and selector data is processed by a front panel CPU that interfaces with the master microcomputer over the instrument bus. The master microcomputer receives and sends all of its information over the instrument bus to the internal circuits. It communicates with the outside world through the GPIB to the IEEE Std 488 connector or through the Accessories Interface to the Accessories connector located on the rear panel. Control language corresponds to front-panel nomenclature of the 494/494P Spectrum Analyzer.

Power Supply Section

The power supply section provides regulated dc power and forced air cooling for all circuits within the instrument. The switching supply is capable of providing regulated voltages over wide input line frequency and voltage ranges. The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all section of the instrument in proportion to the heat generated by circuits within that section. Internal temperature variation is small so as to provide reliable operation.

Other Sections

Signal, power, and control lines between circuit boards and assemblies interconnect through a common Mother board. Most circuit board assemblies plug onto the the top side of the Mother board, assemblies or modules, such as oscillators, of the RF deck, plug through cables and connectors to the bottom side of the Mother board.

Timer (Running time indicator)

An electromechanical timer (M1019) is installed on the Z-Axis board. This timer is calibrated for a duration of 5000 operating hours. Current through the timer causes a copper band to progress along a scale to indicate operating hours.

For Further Information

The circuits that make up the different sections of the 494/494P are described under headings that correspond to those shown in the Functional Block diagram. Detailed block diagrams of these main sections follow the Functional Block diagram. All diagrams are located in the Diagrams section of Volume 2. Detailed block diagrams and circuit schematics of each circuit board and assembly within a section follow the breakdown of the sections.

Circuit theory of operation is described under the Detailed Description that follows. Adjacent to each schematic is a detailed block diagram and a parts location illustration with look-up tables. The parts location illustration and look-up tables should aid in finding components on either the schematic or parts location illustration.

DETAILED DESCRIPTION

The following description is arranged by sections or systems; such as 1st Converter, 2nd Converter, etc., followed by circuit analysis of the circuits within that section. Each system/section is introduced with a description of the system using the system block diagram found in the Diagrams section of the manual. This is followed by a description of each circuit board or major circuit within the system. Adjacent to the title of each section or part is the diagrams number.

1ST CONVERTER ASSEMBLIES ◇2◇ ◇12◇

The 1st Converter consists of the following assemblies: The 0-60 dB Step Attenuator, the Filter Select switch, a 2 GHz Limiter and 1.8 GHz Low-Pass Filter, a 1.7 to 21 GHz Preselector, the Mixer, the 1st LO and Power Divider, Transfer Switch, 2.072 GHz Directional Filter, Diplexer and two 4.5 GHz Low-Pass Filters. External circuits that control or drive the assemblies within the 1st Converter are; the Preselector Driver, 1st LO Driver, Microwave Counter and Phase Lock system, and the RF Interface board.

The 1st Converter converts the incoming RF signals to the 1st IF. Incoming signals are applied through a calibrated 0-60 dB decade attenuator to a filter select switch. Signals within band 1 (10 kHz-1.8 GHz) are routed through a limiter and 1.8 GHz low-pass filter to the mixer, signals within bands 2 through 5 (1.8-21 GHz) are routed through a tunable preselector to the mixer. The RF signals are mixed with the output from a tunable (2.072-6.329 GHz) local oscillator to generate modulation products at the intermediate frequency in use.

The output of the 1st mixer is applied,through Transfer Switch S13, to a directional filter which separates intermediate frequencies 2.072 GHz and 829 MHz for the 2072 MHz 2nd Converter or 829 MHz 2nd Converter. The 2072 MHz IF is applied through a 4.5 GHz low-pass filter to the 2072 MHz 2nd Converter to reject the re-entrant modes of the directional and four cavity band-pass filters. The 829 MHz IF is fed through a diplexer and a 4.5 GHz low-pass filter before it is applied to the 829 MHz IF stages. The 4.5 GHz filter is used to reject re-entrant modes of the 829 MHz band-pass filter internal to the 829 MHz 2nd Converter.

An EXTERNAL MIXER port permits an external mixer to be connected to the instrument to serve as the 1st IF source. The IF signals from external mixers are routed through the Transfer switch to the Directional Filter. This feature is primarily for use with waveguide mixers.

Two intermediate frequencies (2072 MHz and 829 MHz) are used in the analyzer to prevent baseline rise caused by local oscillator feedthrough and crossover of intermodulation products. The 2072 MHz IF is selected for bands 1 and 5, plus the waveguide bands. 829 MHz IF is selected for bands 2-4.

RF Interface Circuits ◇28◇

The RF interface circuits receive instruction from the microcomputer and produce control voltages that drive the RF Attenuator, the Transfer Switch, and the IF Select. These circuits are located on the Z-Axis board and their operation is described under the Z-Axis board part of the Display section.

RF Signal Path ◇12◇

The 0-60 dB Step Attenuator consists of 10 dB, 20 dB, and 30 dB sections which are controlled by relays that are actuated by voltages from the RF Interface circuit.

Coaxial relays S11 and S12 select either the low-pass filter (FL10) and limiter or the Preselector and 3 dB attenuator (AT11) for the RF signal path. The relay coils are driven by circuitry on the Preselector Driver board. The low-pass filter path is used for band 1, band 2 through 5 (signals with frequencies 1.7 to 21 GHz) are routed through the Preselector.

The 2 GHz Limiter operates from 100 kHz to 2 GHz. It has a linear two-port transfer characteristic of unity (−1 dB) until the input exceeds +5 dBm. Above this point, the internal detector diodes conduct, reflecting part of the RF input energy back to the source. As the input level rises, the Limiter reflects more signal, limiting the amount that can pass through the mixer, thus protecting the mixer from burnout.

The 1.8 GHz low-pass filter (FL10) strips the incoming signal of any frequencies above 1.8 GHz and passes the signal below 1.8 GHz to the output segment of selector switch S11.

The Preselector is a 1.7-18 GHz YIG filter that provides high selectivity and image-frequency rejection. Tuning current, which is near 500 mA at 21 GHz, is provided by the Preselector Driver circuits. The Preselector operates on bands 2, 3, 4, and 5. The signal from the Preselector passes through a 3 dB attenuator to the output section of the Filter Selector switch. The Preselector is sensitive to output load impedance so an attenuator is used to help isolate this loading.

1st Mixer

The 1st Mixer is a single balanced design. This has less conversion loss, in comparison to an unbalanced mixer, and this design also cancels local oscillator feedthrough to the RF port. The local oscillator input is split through a broadband multi-section coupler whose outputs are equal in power but 90° out of phase. An additional 90° phase shift is cascaded with the appropriate signal to create a 180° phase difference that is applied across a pair of series-con-

nected Schottky diodes. The result is that the diodes are alternately switched on and off as the local oscillator cycles.

The node between the two diodes is isolated from the 1st LO input by about 30 dB so the RF input is applied to this node. The blocking capacitor at the input connector permits broadband signal application from the RF port, while blocking the dc diode bias to the RF port and the analyzer input. Dc bias for the mixer is via the Transfer Switch, Directional Filter, Diplexer, and 4.5 GHz Filter through the 829 MHz IF circuits. Bias return is through assembly A11 to ground. Bias is supplied from the 1st LO Driver board.

Not counting the IF filtering circuitry, the fundamental conversion loss of the 1st Converter is about 14 dB; third harmonic conversion loss is about 24 dB. The Schottky diodes are mounted in a sub-assembly of the mixer so they can be easily replaced.

1st Local Oscillator

The 1st LO is a YIG (Yitrium-Iron-Garnet) oscillator that has a tuning range of 2.072 to 6.35 GHz. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The $+15\ V_1$ voltage provides operating bias for the oscillator. The supply is protected and decoupled by VR1010, C1016, and R1011. The second supply, $+15\ V_2$, is for future applications. VR1018 and VR1019 clamp transient voltages from the tune voltage coil. It also protects the driving circuits from the transients induced when degaussing.

Relay K1015 is closed when the FM coil is used to sweep the oscillator. C1012 and C1014 are connected across the tune coil to lower the noise bandwidth of the main coil driving circuit while the FM coil is in operation. The heater provides temperature stability.

Power Divider (A13)

The Power Divider splits the output of the 1st LO (YIG oscillator) to isolate the 1st Mixer from the 1st LO OUTPUT front panel connector. The unit is essentially two multi-section directional couplers that are multi-port cascaded to produce two ports having equal power. The isolation between output ports is 15 dB or more at the operating frequency. The Power Divider also provides an improved load to the local oscillator.

Transfer Switch

The Transfer Switch is a three-port coaxial switch that permits application of 1st IF signals from inside or outside the analyzer. This allows the use of an external mixer by bypassing the 1st Converter circuitry. The function is controlled by circuitry on the RF Interface board. It is automatically actuated when waveguide bands are selected or the front panel EXT MIXER push button is pressed.

Directional Filter

The Directional Filter (FL16) couples the 2072 MHz signal to the 2nd Converter via low-pass and band-pass filters,FL11 and FL14. As mixing products pass through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to the low-pass filter FL11. The remainder of the IM products pass on through, since the ring is excited only with 2072 MHz signals. The bandwidth of this unit is approximately 45 MHz. The unfiltered signals are passed on to the Diplexer.

2072 MHz IF Filters

The 2072 MHz signal, from the Directional Filter, passes through a low-pass filter (FL11) which rejects all signals above 4.5 MHz. The signal is then sent through a 15 MHz band-pass filter (FL14) which rejects IM products either side of the 2072 MHz IF.

Diplexer and Filter

The Diplexer (A14) passes the 829 MHz IF signal from the mixer output through a low-pass filter (FL15) to the 2nd Converter. The Diplexer and directional filter provide a broadband impedance match to the 1st Mixer IF port. This match contributes to the overall flatness and frequency response of the analyzer.

2ND CONVERTER CIRCUITS (12)

Two 2nd Converter systems are used in the 494/494P Spectrum Analyzer. One converts 2072 MHz to 110 MHz and the other converts 829 MHz to 110 MHz. The operation of either converter is a function of the selected frequency band. The IF selection for each band is shown in Table 7-1 along with the center frequency range and the local oscillator frequency range. Two 2nd IF's are used by the analyzer for the following reasons:

1. If a frequency band were to include the first intermediate frequency within its range, it is possible for some input signals to pass through the Preselector and the 1st Converter (without conversion), into the 2nd Converter at the 1st intermediate frequency. The resultant spurious signal will cause the baseline level on the screen to rise and obscure real signals. By the use of two 2nd converters, the analyzer can overlap frequency bands so they do not include the first intermediate frequency, and avoid this problem.

2. With two IF'S, IF feedthrough in band 2 and higher order spurs in bands 3 and 4 can be eliminated.

3. Because of the limited tunning range of the 719 MHz LO, the lower IF cannot be used above band 4.

The 2072 MHz 2nd Converter mixes the 2072 MHz from the 1st Converter with the output from a 2182 MHz phase-locked 2nd local oscillator. This local oscillator is swept and tuned over a 4 MHz range. The 2072 MHz input IF signal is passed through a four-cavity band-pass filter (FL14) to allow only the 2072 MHz 1st IF signal to pass through and prevent other signals, generated within the 2nd Converter, from getting back to the 1st Converter. A diode mixer combines the 2072 MHz IF input and the local oscillator signals to generate the 110 MHz IF output which then passes through a 110 MHz low-pass filter to reject any higher order signals from the mixer.

The 829 MHz 2nd Converter uses a phase-locked voltage controlled oscillator to produce the 719 MHz signal that is mixed with the 829 MHz first IF signal. The swept 2182 MHz 2nd Local Oscillator is used as a reference for the phase locked oscillator. The 719 MHz oscillator can be disabled upon command from the microcomputer in the IF selection process. The phase lock circuit maintains a constant relationship between the two local oscillators as the 719 MHz oscillator is swept and tuned over a 1.33 MHz range. A four section coaxial band-pass filter is used before the mixer to exclude any RF signals other than the desired 829 MHz . Again, a diode mixer is used to mix the 829 MHz input and local oscillator signals to produce the 110 MHz second IF output.

Selection between the two IF signals also takes place within the 829 MHz converter system. Under command of the microcomputer (by way of the RF Interface circuits) a diode selector switching network connects one of the two 110 MHz second IF signals to the output for application to the 3rd Converter.

Table 7-1
2ND CONVERTER IF SELECTION

Frequency Band	Center Frequency Range	2nd Local Oscillator Frequency (MHz) Range	Converter System IF
1	0-1.8 GHz	2182 ±2.25	2072 MHz
2	1.7-5.5 GHz	719 ±0.75	829 MHz
3	3.0-7.1 GHz	719 ±0.75	829 MHz
4	5.4-18.0 GHz	719 ±0.75	829 MHz
5	15.0-21.0 GHz	2182 ±2.25	2072 MHz
6	18.0-26 GHz	2182 ±2.25	2072 MHz
7	26-40.0 GHz	2182 ±2.25	2072 MHz
8	40.0-60.0 GHz	2182 ±2.25	2072 MHz
9	50.0-0.0 GHz	2182 ±2.25	2072 MHz
10	75-40.0 GHz	2182 ±2.25	2072 MHz
11	110-220 GHz	2182 ±2.25	2072 MHz
12	170-325 GHZ	2182 ±2.25	2072 MHz

2072 MHz 2ND CONVERTER (12)

The 2072 MHz 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a low-loss, narrow band, four-cavity filter, connected, through an external cable, to a low conversion loss narrow band diode mixer, a 110 MHz low-pass filter, and a mixer biasing circuit that will disable the mixer when directed by the microcomputer.

Four-Cavity Filter

The four-cavity (band-pass) filter, which is depicted on Diagrams 11, 12, and 13, is designed to pass only the 2072 MHz IF signal to the mixer and to reflect any other frequencies back to the 1st Converter for termination. In addition, the filter keeps the converter LO and mixer products from entering the 1st Converter.

This filter has a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat plugged into a 3 millimeter connector. Intercavity coupling is provided by coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the filter top, and is fine tuned with a tuning screw on the side of each cavity. All of the tight machining tolerances are confined to the top. Thus, the main cavity milling need not be a high precision part. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end (in a 50 Ω system). Figure 7-1 shows a cross sectional view of the filter; Figure 7-2 shows the equivalent electrical circuit.

Mixer Circuit

The mixer circuit in the 2072 MHz 2nd Converter is of the single-balanced, two diode type. It consists of the mixer, an operational amplifier bias circuit, a delay line, and a low-pass filter. In opertion, both diodes of the mixer are turned on and off by the output signal from the 2182 MHz 2nd Local Oscillator through coaxial connector P183. Although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180° phase shift delay line in the input line to the upper deck. Note that the diodes are matched and must be replaced as a pair if one fails.

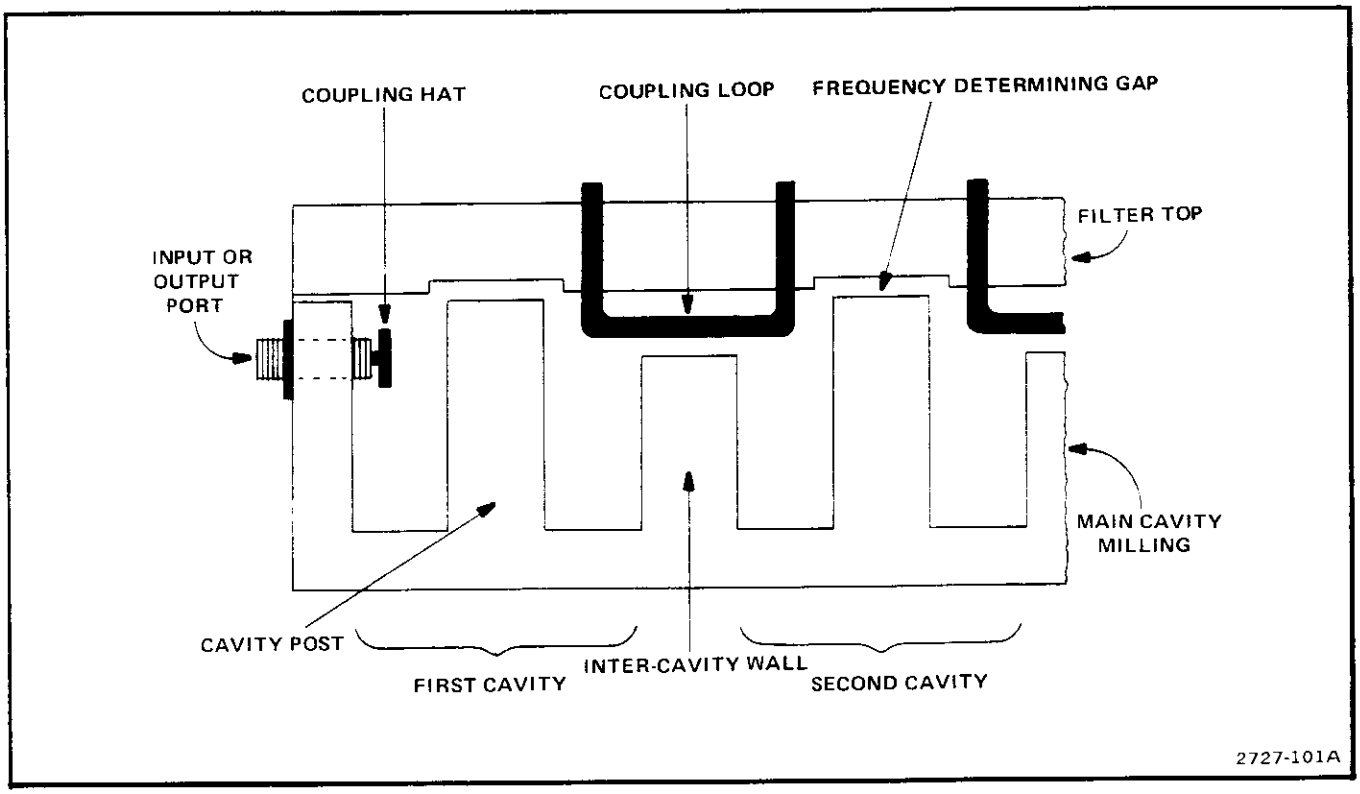


Figure 7-1. Cross section of a four-cavity filter.

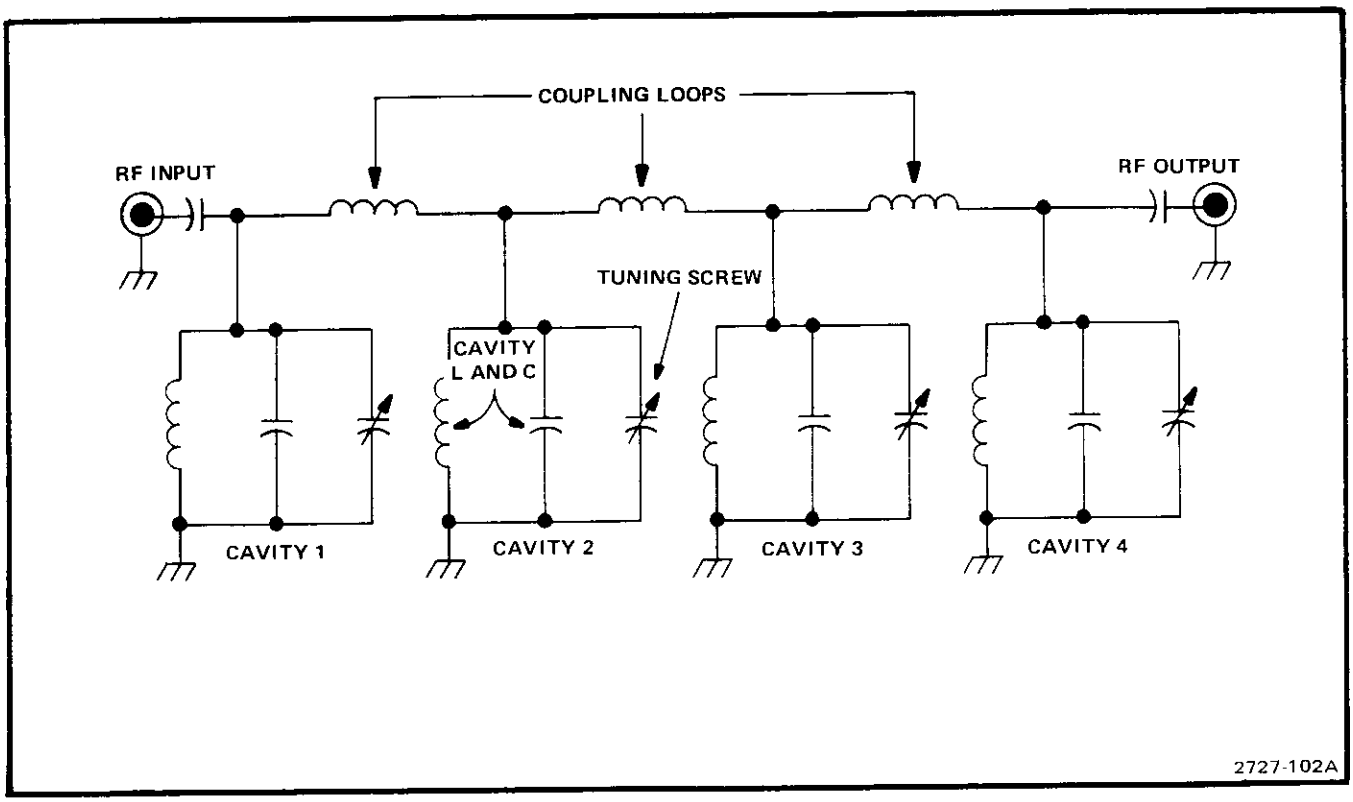


Figure 7-2. Equivalent circuit of the four-cavity filter.

2072 MHz RF from the four-cavity filter (FL14) enters the mixer, where it is switched on and off at a 2182 MHz rate by the mixer diodes. Conduction of the diodes is controlled by the much stronger 2182 MHz LO signal. Several mixing products result; one, the difference frequency of 110 MHz is separated from the others by a low-pass filter for use as the IF output.

The two inductors and one capacitor, at the output of the mixer, form a low-pass filter that passes 110 MHz unattenuated to the 829 MHz 2nd Converter, via coaxial connector P182. Capacitors, at each of the three inputs to the mixer, keep the diode bias from being impressed upon the RF and local oscillator lines.

The bias circuit, which consists of operational amplifier U1014 and the associated components, establishes the bias for the mixer diodes and also provides the means for effectively switching the mixer off (under control of the microcomputer). When the mixer is active, each diode has approximately 2 mA of forward bias. For this condition, the IF SELECT signal from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from U1014A to be at +14 V and the output from U1014B to be −14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 plus resistor R1014, and potentiometer R1010 plus resistor R1017, provide forward bias to the diodes. The potentiometers are set to balance the bias levels.

In operation where the mixer is not active, the IF SELECT signal is high. This reverses the states of the U1014 outputs and forward-biases diodes CR1014 and CR1018. With these diodes conducting, resistors R1014, R1016, R1017, and R1018 form two voltage dividers that set the reverse bias, to the mixer diodes, at 5 V. This effectively turns the mixer off and attenuates the 110 MHz signal by about 55 dB.

Precision External Cables

The external cable that connects the four-cavity filter output to the mixer circuit and the external cable that connects the 2nd local oscillator to the mixer circuit are both critical length cables.

The Four-Cavity Filter-to-Mixer Input Cable (W140). Several products and harmonics of the local oscillator and RF input frequencies will exit the mixer via the RF input port of the mixer. The image (RF input minus the 2nd LO) and the sum (RF input plus the 2nd LO) are two significant products. There is enough energy in these two signals to warrant efforts to recover that energy.

Only the RF signal at 2072 MHz can pass through the four-cavity filter. Thus, any other signal frequency that is applied to the filter (that is, signals exiting the mixer via the RF port) is reflected back to the mixer by the filter. If the cable between the filter and the mixer is the correct length, the most significant reflected signals (that is, the image and the sum) can be returned to the mixer in phase and converted into additional energy at the intermediate frequency. This technique is called "image enhancement mixing" and typically improves conversion loss by approximately 3 dB at the design frequencies.

The image frequency, in this instance, is very near the RF frequency. A very sharp cut-off filter is required to pass the RF, yet reflect the image. The four-cavity filter performs this function.

The 2nd Local Oscillator-to-Mixer LO Input Cable (W222). The image and sum products are also present at the LO port of the mixer. These signals leave the mixer via the cable to the 2nd LO and are reflected back to the mixer by the LO The oscillators resonator appears highly reflective to the image and sum signals because it is tuned to the LO frequency. Again, the length of the cable from the LO to the mixer LO port is adjusted so the image and sum signals are reflected back to the mixer, in the proper phase, for reconversion to supply additional energy at the IF frequency.

2182 MHz PHASE LOCKED 2ND LO

◈13◈ ◈14◈

General Description

The 2182 MHz phase locked 2nd LO assembly contains a tunable microwave oscillator, frequency reference, and phase lock circuitry within a two-section housing. Microwave circuitry is packaged within the machined aluminum portion of the housing. Low frequency phase lock circuitry is within the mu-metal compartment.

In the microwave or LO portion of the assembly, the 2182 MHz Microstrip Oscillator generates 2182 MHz for the 2nd converters and the 2nd LO internal reference circuitry. The 2200 MHz Reference circuit receives a 100 MHz drive signal from the 3rd converter crystal oscillator and produces 100 MHz harmonics. The 22nd harmonic or 2200 MHz is mixed with 2182 MHz from the microstrip oscillator in the 2200 MHz Reference Mixer circuit. The difference frequency of 18 MHz is then fed to the phase lock side of the module.

A phase/frequency detector, on the 16-20 MHz Phase Lock circuit board, compares the 18 MHz difference frequency with a signal from a linearized varactor tuned, 18 MHz voltage controlled oscillator. The detector output tunes the 2182 MHz Microstrip Oscillator such that the difference frequency exactly matches the frequency of the 18 MHz reference VCO.

Sweep and tune signals from the Span Attenuator and Center Frequency Control circuits tune the 18 MHz VCO. The output voltage from the phase/frequency detector forces the Microstrip Oscillator to tune the same amount.

2182 MHz Microstrip Oscillator ◈13◈

This oscillator consists of a printed half wavelength resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer, connected between the base and collector of Q1021. Part of the base feedback capacitance is provided by a bendable tab (C1021). This allows fine adjustment of the total feedback. This feedback RF signal is detected, by the base-emitter junction of Q1021, to produce a change in bias voltage that is related to the amount of feedback. The base voltage can be monitored at TP1015 with a high impedance voltmeter without significantly disturbing the oscillator.

The dc collector voltage and current for Q1021 is regulated by an active feedback circuit containing transistor Q2021. Voltage at the junction of R2023 and L2023 is a function of Q1021 collector current. This voltage is sensed by Q2021, which alters the base current to Q1021 thereby regulating the collector current and maintaining +10 V dc on the resonator. Decoupling and control of bias loop dynamics are provided by C2104. Resistor R2016 swamps the negative base resistance of Q1021 to provide stabilization. Resistor R2015 protects the base-emitter junction of Q1021 from excessive reverse bias in the event the +12 V supply fails.

The oscillator is tuned by varactor diode CR1028, connected to one end of the resonator. Decoupling for the varactor is provided by the low-pass elements in the tune line. Bendable tab C1022 can be used to fine tune the oscillator center frequency.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One output supplies 2182 MHz through a 6 dB attenuator to the Harmonic Mixer in the 829 MHz 2nd Converter. The other two output taps couple LO power through 6 dB attenuators to buffer amplifiers Q1031 and Q1011. The amplifiers provide approximately +10 dBm to the 2072 MHz 2nd Converter and +8 dBm to the Reference Mixer.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by a single

common-emitter transistor (Q1011). Printed elements provide input and output impedance matching. Out-of-band damping is provided by R1011 in series with a 1/4 wavelength shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wavelength open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use nor need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wavelength shorted stub, and R1011. The 1/4 wavelength shorted stub is grounded through C2011 (C2011, C1013, and L1011 are also used for decoupling). Collector voltage is determined by divider R1013 and R2013; this controls the dc feedback to the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. Diode CR2013 protects the base of Q1011 from excessive reverse bias if the +12 V supply fails.

2200 MHz Reference Board ◈13

This circuit generates harmonics of the 100 MHz input. The 22nd harmonic or 2200 MHz is used by the Reference Mixer. The input 100 MHz signal is applied through a matching network (consisting of L1034, L1025, C1036, C1029, and C1025) to a differential amplifier (Q1024 and Q2024). The emitters of this amplifier are ac coupled through C2026, reducing low frequency gain and ensuring balanced operation. A snap-off diode (CR2014) is driven by the amplifier, via transformer T2015, to generate multiple harmonics of the 100 MHz signal including the 2200 MHz reference. The output passes through a 3 dB attenuator, for isolation, to the Reference Mixer circuit.

2200 MHz Reference Mixer ◈13

Signals from the 2200 MHz Reference circuit are filtered by a printed 2200 MHz bandpass filter. Diodes CR1011 and CR1012 are the switching elements of a single-balanced mixer. The microstrip oscillator output is applied to CR1011 and through a half wavelength delay line to CR1012. The delay line shifts the oscillator signal 180° so both diodes switch together. Mixing the 2200 MHz with the oscillator 2182 MHz signal produces the difference frequency of 18 MHz. This 18 MHz signal is fed through a 37 MHz low-pass filter to the 16-20 MHz phase lock circuit. The low-pass filter prevents unwanted products, such as 82 MHz (product of 2100 MHz and 2182 MHz), from passing into the phase lock circuit.

16–20 MHz Phaselock Board ◈14

This board contains regulated power supplies, a 16-20 MHz (18 MHz nominal) voltage controlled oscillator with linearizing circuitry, and a phase/frequency detector circuit. Its main function is control of the 2182 MHz Microstrip Oscillator. The entire circuit board is housed in a magnetic shield to reduce spurious effects of external ac fields. All power supply and control inputs enter the circuit board via feedthrough capacitors in the housing wall. All connections with the microwave circuitry are through feedthrough capacitors C2200-C2204, in the floor of the housing.

The +15, −15, and +9 V supply inputs are re-regulated down to +12, −12, and +5.2 V by regulators using quiet operational amplifiers. IC U2025 provides a stable −6.2 V reference that is filtered by R2018 and C2015 and amplified by U2016B to produce the −12 V supply. IC U2016B uses emitter-follower Q2024 to increase the current capability of the supply. Resistor R2013 ensures sufficient base drive, while collector resistor R2025 reduces power dissipation in Q2024. Diode CR2019 protects the base-emitter junction during power supply shutdown. Feedback resistors R2016 and R2017 set the gain of U2016B and control the −12, +12, and +5.2 supply voltages. The −12 V supply is applied to inverting amplifier U2016A to produce the +12 V supply, and inverting amplifier U1017 to produce the +5.2 V supply. The output circuitry for the +12 V and +5.2 V supplies are similar to the −12 V supply.

Differential amplifier U2072A accepts the 2nd LO sweep voltages. One input senses the sweep voltage while the other input senses the ground potential at the Sweep board. Sweep sensitivity is adjusted by selecting resistor R2070. In wide spans, the sweep signal passes through parallel resistors R2082 and R2083. In narrow spans, R2082 may be switched out by Q2084, which reduces the sweep sensitivity by a factor of ten. When the TTL signal to Q2076 is high, Q2076 is turned off, R2086 holds the gate of Q2084 to −15 V, Q2084 is turned off, and R2082 is switched out. This reduces the sweep sensitivity. When the TTL signal is low, Q2076 saturates with the collector slightly above 0 V, Q2084 turns on, and full sweep sensitivity is restored.

Amplifier U2072B accepts the 2nd LO tune voltage. the Tune board senses the ground potential of the 16-20 MHz Phase Lock board and floats the tune voltage. Tune sensitivity is adjusted by selecting resistor R2072.

The sweep and tune signals combine at the summing node input of a non-linear shaping amplifier. The non-linearity of the shaping amplifier compensates for the non-linear tuning of the reference oscillator varactor to give a linear tuning characteristic from 16 to 20 MHz. The shaping function is produced by a resistor-diode array in the feedback loop of inverting amplifier U1073A.

All of the amplifier's feedback is through R1072 when the output swings to the negative limit. As the output voltage swings less negative, it sequentially passes the tap-point voltages of a series of voltage dividers connected between 0 V (the summing node at pin 12) and a negative reference set by Q1047. If the output becomes positive with respect to a given divider tap, a corresponding diode in U2059 for-

ward biases and connects the output to the tap, which creates additional feedback through one leg of the divider to the summing node. This causes R2051, then R2052, then R2053 (as so on through R2056) to be connected in parallel with R1072 as the amplifier output becomes less negative. This progressively increases the feedback, which causes the gain of U1073A to decrease.

Another series of dividers connected between the amplifier's output and a negative voltage reference causes the diodes in U1059 to sequentially conduct as the output becomes more positive. Resistors R2060, then R2061, then R2062 (as so on through R2065) are sequentially added in parallel with the existing feedback. Soft diode turn-on characteristics and a large number of breakpoints result in smooth gain changes. The non-linear amplifier's voltage-gain characteristic is controlled by the shaper reference voltage, which is set by R2049. Altering R2049 will make the breakpoints either closer together or further apart; in practice, this resistor is selected to correct the tolerance variations of the 18 MHz VCO varactor.

The forward drop of the shaper diodes gives U1073A an offset voltage. Temperature correction diodes CR1086, CR1087, and CR1088 correct this offset over a wide temperature range by summing a correction voltage through R1074. These diodes also compensate for the lack of series diode drop across R1072 and eliminate offsets at the summing input of U1073B. Selecting R1070 provides fine adjustment of the VCO's center frequency. IC U1073B is an inverting amplifier that increases the shaper output voltage swing to a level that can control the varactor of the 18 MHz VCO.

A differential amplifier with well-defined limiting characteristics is used for the 18 MHz VCO. Emitter degeneration is used to control loop gain. Transistors Q2096 and Q2087 form the differential pair of transistors, with the emitters coupled through C2091. Transformer T2092 provides ac feedback for the collector-base junction of Q2096 and also creates the majority of the resonator inductance. The total resonator inductance may be adjusted by trying different combinations of connections between taps on inductor T1091 and transformer T2092. These taps allow coarse adjustment of the VCO center frequency. The capacitor of the resonator is varactor CR1089. Capacitor C1088 completes the resonator ac path and acts as a dc block, which allows a bias voltage to be impressed on the varactor. Resistor R2092 and capacitor C2090 damp the Q2096 collector, which prevents high-frequency instability in the oscillator. Transistor Q2087 provides a buffered oscillator output.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the 18 MHz signal from the 2200 MHz Reference Mixer board. Transistor Q1041 is the common-emitter first stage while Q1042 and Q1043 form the differential second stage. The differential stage limits the output swing to 0.8 V to prevent over-driving the following ECL circuitry. Dc bias is maintained by Q1041, which has dc collector-base feedback via R1046 and the R1043/R1048 voltage divider. Transistor Q1043 receives its base bias through R1042. Each transistor operates with 5 mA of quiescent current.

ECL line receivers U2041D and U2041B amplify and buffer the 18 MHz signals from the Reference Mixer and the VCO, respectively. These two signals are then applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops, U2031A and U2031B, comprise the phase/frequency detector. The flip-flops drive a common reset line with a wired-AND output. The clock input of U2031B is driven with the signal from the 18 MHz VCO, and the clock input of U2031A is driven with the signal from the 18 MHz signal from the Reference Mixer.

Both flip-flops are configured to reset together whenever both are set. If they are clocked with signals that exactly match in frequency and phase, then both flip-flops set simultaneously and then almost immediately reset. If the Reference Mixer signal has a slight phase lead, U2031A will remain set longer than U2031B. If the Reference Mixer signal has a slight phase lag, U2031B will set first and remain set the longest. The signal that has the phase lead will cause the associated flip-flop to be set a greater percentage of time than the lagging flip-flop. If there is a frequency difference between the two inputs, the flip-flop with the higher input frequency will be set more of the time than the other flip-flop. The ratio between the filtered output signals of the two flip-flops indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 18 MHz VCO signal.

The outputs of the flip-flops are low-pass filtered by C1031 and C1028 and applied to differential amplifier U1031. U1031 compares the outputs of the flip-flops and produces an output that controls the tuning of the 2182 MHz microstrip oscillator. The phase-lock loop bandwidth is controlled by R1026, C1029, R1027, and C1026. The gain slope breaks to -12 dB/octave for frequencies below 16 kHz. Resistors R1033 and R1034 divide and offset the output of U1031 so the tune voltage ranges between 0 and -12.5 V.

The output of divider R1033/R1034 is applied to the varactor of the 2182 MHz microstrip oscillator (2nd LO). This closes the phase-lock loop, tuning the 2nd LO so that it closely tracks the 18 MHz VCO. When the 18 MHz VCO is tuned, U1031 simultaneously tunes the microstrip oscillator an equal amount. Within the loop bandwidth, the 2nd LO performance is determined by the 18 MHz VCO instead of

the microstrip oscillator, giving a significant improvement in frequency stability and reduction of phase noise.

829 MHz 2ND CONVERTER

If Section 15 16 15

The 829 MHz 2nd Converter down-converts the 829 MHz signal from the 1st Converter to 110 MHz for application to the 3rd Converter and provides the switching capability for the microcomputer controlled selection of either the 2072 or the 829 MHz converter system. The converter circuits consist basically of an input diplexer, an amplifier, a band-pass filter, a mixer, and a diode switch.

829 MHz Diplexer Circuit 15

The diplexer passes signals at 829 MHz with minimum attenuation (approximately 1 dB) and has a pass-band of approximately 200 MHz. All frequencies outside the pass-band, from approximately 50 kHz to 2 GHz, are terminated in 50 Ω loads with a match of at least 10 dB. Figure 7-3 shows a simplified schematic of the diplexer.

At 829 MHz, the series resonators provide a low impedance path from input to output. (Note on Diagram 15 that the input is from the 1st Converter through coaxial connector P231.) Ideally, signal loss across the 50 Ω resistors is zero because of the low impedance path around these resistors. The parallel resonator appears as an open circuit at 829 MHz.

At frequencies above or below the pass-band, the series resonators appear as large reactances, shifting the primary signal flow through the 50 Ω resistors. The out-of-band impedance of the parallel resonator is now small compared to 50 Ω. Thus, the resistors are essentially grounded at one end, terminating both the input and output ports. A wide bandwidth is used to minimize loss in the resonators and eliminate adjustments. Relative bandwidths of the series and parallel resonators are optimized to provide reasonable match at the band edges.

As shown in Diagram 15, the diplexer contains components not shown in Figure 7-3. Two pairs of 100 Ω resistors (R1012/R1015 and R1011/R1012) are used in parallel to form each 50 Ω termination. This reduces load inductance. A small capacitor is connected across each load (C1010 and C1013) to improve impedance match at frequencies above the pass-band. The inductor in the parallel resonator is a printed length of transmission line that is tapped to establish the correct bandwidth. One end of this inductor is grounded through four capacitors (C1017, C1016, C1019, and C1018) so that dc bias from the 1st Local Oscillator Driver can be introduced to the mixer through the diplexer. Four capacitors are used in parallel to minimize inductance variations

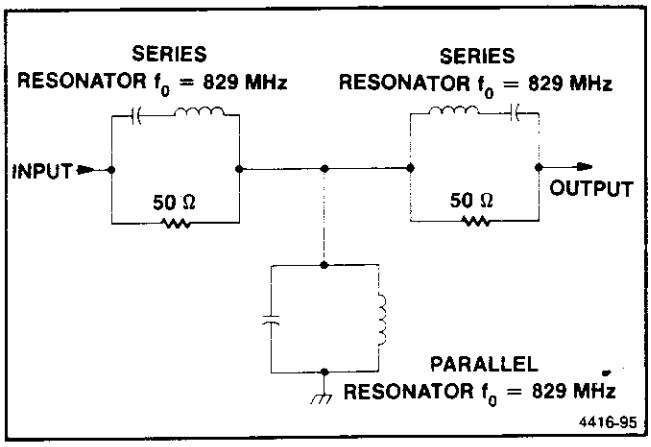


Figure 7-3. Simplified diagram of the diplexer.

and circuit Q degradation. A low-pass filter is included in the bias line to keep noise from the 1st Converter.

The diplexer is followed in the signal path by a printed circuit five-element low-pass filter that consists of three shunt capacitors and two series inductors. Cutoff frequency for this filter is approximately 1.2 GHz.

829 MHz Amplifier Circuit 15

The 829 MHz Amplifier provides approximately 18 dB of signal gain at 829 MHz and consists of two nearly identical amplifier stages in cascade (Q1017 and Q1025), plus a 3 dB attenuator. The overall noise figure is approximately 2.8 dB. The gain stages are designed as general purpose, unconditionally stable amplifiers for use in a 50 Ω system. Operation of a stage is covered by describing the ac and dc signal paths separately. Figures 7-4 and 7-5 are simplified diagrams of the ac and dc signal paths.

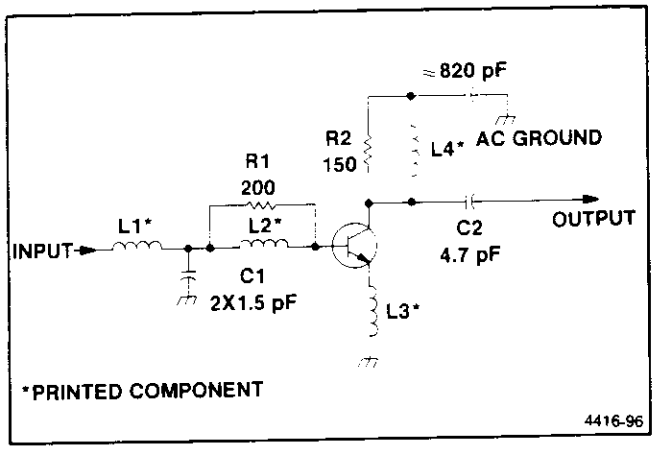


Figure 7-4. Equivalent ac circuit of an amplifier stage in the 829 MHz 2nd converter.

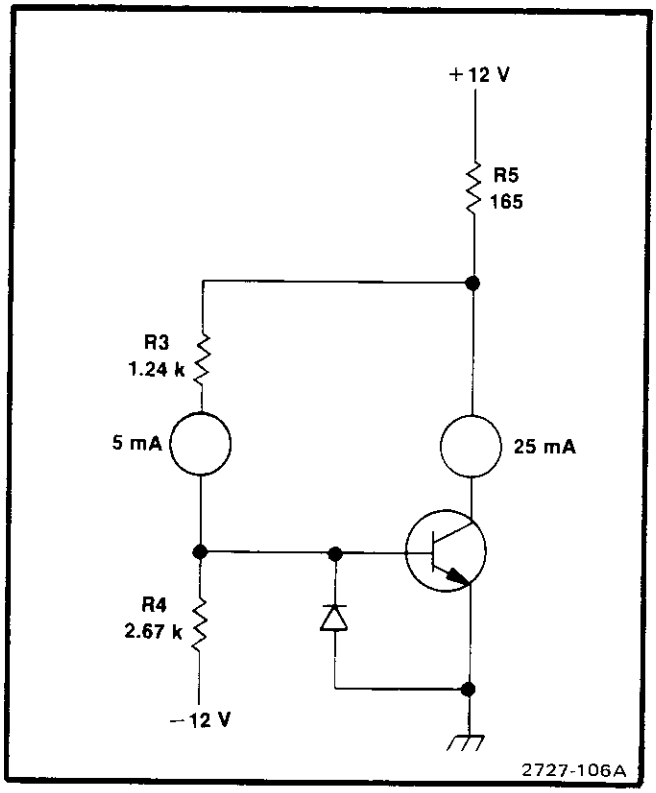


Figure 7-5. Simplified diagram of the dc path in an amplifier stage.

In the ac circuit (Figure 7-4) capacitor C1 and printed circuit inductors L1 and L2 form the input matching network. (In the first stage, inductor L1 is actually the series inductance of dc blocking capacitor C1016.) The collector circuit is matched to 50 Ω by inductor L4 and capacitor C2. Gain is primarily controlled by printed circuit emitter inductor L3. High frequency stability is enhanced by resistors R1 and R2. That is, at frequencies well above 829 MHz, resistor R1 ensures low common-base gain and resistor R2 helps to dampen the collector circuit.

In the dc circuit (Figure 7-5) negative feedback through the voltage divider, consisting of resistors R3 and R4, sets the collector voltage as a fixed proportion of the −12 V reference supply. Collector current is determined by resistor R5. Current requirments for the first stage is less than the requirements for the second because the first stage requires less intermodulation distortion performance. Reverse breakdown of the base-emitter junction can degrade the transistor performance, so a diode base clamp is provided in each circuit (CR1013 and CR1022) to protect the transistor if the +12 V supply should fail.

Not shown in Figures 7-4 and 7-5 are inductor L1014 and a capacitor C1014 in the base circuit for Q1017 and L1021,C1023 for Q1025 plus a capacitor in the collector circuits (C1013 for Q1017; C1027 for Q1025). These decouple the signal path from the bias network.

The 3 dB attenuator (R1026,R1027,R1025, and R1029) helps maintain a wideband 50 Ω interface between the second amplifier stage and the 829 MHz bandpass filter. A test point (J1029) at the output of the attenuator is used to verify amplifier performance and to aid in adjustment of the following 829 MHz band-pass filter. From the attenuator, the signal is applied to the 829 MHz 2nd Converter Mixer circuit.

829 MHz Mixer Circuits

Frequency conversion from 829 MHz to 110 MHz occurs on the 829 MHz 2nd Converter board. The board contains a coaxial band-pass filter, a 1.3 GHz low-pass filter, a 3 dB attenuator, and a two-diode, single-balanced mixer with associated frequency diplexing circuitry.

829 MHz 1st IF signals, from the 829 MHz Amplifier, enters the converter through an 829 MHz band-pass filter. The filter blocks unwanted inputs, primarily the 609 MHz image signal. A 1.3 GHz printed element low-pass filter blocks high frequency signals that would otherwise be admitted at the re- entrant frequencies of the band-pass in excess of 2 GHz. The function of the 1.3 GHz low-pass filter is shared by the 1.2 GHz low-pass filter, located on the 829 MHz Diplexer board. A 3 dB attenuator on the 829 MHz Amplifier board and one following the 1.3 GHz low-pass filter help ensure consistent 50 Ω interfaces for the 829 MHz band-pass filter.

The 829 MHz band-pass filter consists of four, quarter-wave, coaxial type resonators, mounted on the 829 MHz 2nd Converter board. The end resonators are tapped near their grounded end to facilitate the filter's input and output coupling. Inter-resonator coupling is provided by printed "through-the-board" capacitors that connect between the resonators at their high impedance end. A bendable tab is located at the high impedance end of each resonator for fine adjustment of resonant frequency. The bendable tab acts as a small, variable capacitance from the end of the resonator to ground, making fine adjustments of resonant frequency possible. When properly tuned, the filter presents an input return loss of at least 12 dB at 829 MHz and an insertion loss of about 2 dB.

829 MHz enters the mixer diodes through a 450 MHz high-pass filter. The high-pass filter blocks the lower IF signals generated within the mixer. The mixer diodes are transformer driven by a large amplitude (+12 dBm) 719 MHz from the local oscillator. This large signal drives the diodes in and out of conduction and switches the smaller 829 MHz signal on and off, at a 719 MHz rate, to generate several IM products.Only the difference frequency of 110 MHz is allowed to leave the mixer by way of a 300 MHz low-pass

filter which blocks LO, RF, and higher frequency products. The sum product of 1548 MHz, is reflected back to the mixer by the 829 MHz band-pass filter, in-phase with LO harmonics, to increase the energy of the 110 MHz signal. A printed delay line, between the 829 MHz band-pass and 1.3 GHz low-pass filters, controls the phase delay. The net result of this "image enhancement" is low conversion loss and good inter-modulation distortion performance. The 3 dB attenuator reduces the image enhancement affect and permits the use of non-critical line lengths and filter characteristics. Overall conversion loss, from 829 MHz to 110 MHz, is about 8.5 dB, including 2 dB from the 829 MHz band-pass filter and 3 dB from the attenuator.

110 MHz IF Select Circuits

The 110 MHz IF Select circuits select the 110 MHz IF signal from either the 829 MHz 2nd Converter or the 2072 MHz 2nd Converter for transmission to the 110 MHz IF Amplifier. The 110 MHz IF signal, from the 829 MHz Converter, is applied directly to the select switch circuit. The 110 MHz IF signal, from the 2072 MHz converter, is applied (via coaxial connector P233) through a controlled amplifier to the select switch circuit. The switch circuit diodes are CR2011, CR2012, CR2013, and CR1015.

When the IF SELECT line to the 829 MHz 2nd Converter (via feedthrough C236) is low, series diode switch CR2011 is turned on. This steers the 110 MHz IF signal, from the 829 MHz 2nd Converter, to the output port. At the same time shunt diodes CR2012, CR2013, and CR1015 turn on and Q1011 turns off to isolate the output port from any spurious signals from the 2072 MHz 2nd Converter.

When the IF SELECT line goes high, amplifier Q1011 turns on and shunt diodes CR2012, CR2013, and CR1015 turn off to allow the 110 MHz IF signal, from the 2072 MHz 2nd Converter, to be applied to the output port. Series diode CR2011 also turns off to prevent signal loss into the inactive 829 MHz 2nd Converter. Isolation for the 829 MHz 2nd Converter is not critical, when the 829 MHz Converter is inactive, because the 719 MHz LO is also turned off by the state of the IF SELECT line.The switch and amplifier logic is summarized in Table 7-2.

As described above, diodes are used as the basic switch elements. When forward biased, with current of several milliamps, the diodes present only a few ohms of series resistance to RF signals. When reverse biased, the diodes present essentially an open circuit. The control signal from switch driver Q2015 is connected in a series path through the four diodes (CR2011, CR2012, CR2013, and CR1015) and inductors L2011, L2013, and L2019 so only a small current is required to forward bias all four diodes. This bias current is also used to turn off Q1011.

Table 7-2
SWITCH AND AMPLIFIER SELECTION SUMMARY

IF Select Line	Series Switch	Shunt Amplifier	110 MHz IF Source
High	On	Off	829 MHz 2nd Conv.
Low	Off	On	2072 MHz 2nd Conv.

Diodes CR2012 and CR2013 are incorporated into a pi-type matching network, consisting of inductors L2011, L2013, and capacitor C2012, so both switches shunt the signal at moderately high impedance points. In addition, when the switch diodes are turned on, parallel resonance, between inductor L2011 and capacitor C2012, presents virtually an open circuit to signals passed by switch diode CR2011. Switch diode CR2013 is located at the high impedance node created by series resonant inductor L2019 and capacitor C2017. Diode CR1015 directly shunts the output from Q1011.

Transistor Q1011 operates as a common-emitter amplifier for the 110 MHz IF signal from the 2072 MHz 2nd Converter. Its gain and impedance match are controlled primarily by feedback resistors R1011 and R1012. Resistors R1013 and R1018 attenuate the output by approximately 6 dB for enhanced control of match and stability characteristics. Dc collector current from Q1011 develops a voltage across resistor R1017. Bias control transistor Q1012 then compares this voltage with the fixed voltage of the voltage divider, R1015 and R1016. Any variation in the collector current of Q1011 is sensed by Q1012 and offset by a resulting change in the Q1011 base current. Collector current for Q1011 is set, in this manner, at approximately 15 mA.

When the control current from Q2015, through the switching diodes, develops a voltage across R1017 that exceeds the control limits of Q1012,it effectively removes the base-bias from Q1011 and turns Q1011 off. Negative current, supplied through resistor R1014, ensures that Q1011 is turned off by the loss of positive base drive. Diode CR1011 protects the base of Q1011 from excessive reverse bias. Voltage across R1017 is approximately 3.4 V when Q1011 is turned on and approximately 4.4 V when it is off. Overall gain is approximately 12.8 dB when the amplifier is turned on.

From the diode switch circuit, the 110 MHz IF signal is transmitted via coaxial connector P232 to the 110 MHz IF Amplifier.

829 MHz 2nd Converter, LO Section (16)

The 829 MHz 2nd Converter LO generates the 719 MHz frequency that is mixed with the 829 MHz IF to produce the 110 MHz IF signal. In the following description, the circuits are referred to as the 719 MHz LO. The 719 MHz LO consists of a phase lock loop, a 719 MHz output circuit, and a 2nd LO front panel output circuit. Refer to Diagram 16 while reading the following description.

Phase Lock Circuit (16)

The phase lock circuit receives reference frequency inputs and uses phase/frequency detection techniques to use those signals in controlling the output frequency of the 719 MHz oscillator. The circuit consists of a voltage controlled oscillator (VCO), a phase/frequency detector, a harmonic mixer, and various amplification stages and power splitters. When the 719 MHz LO is enabled, the 2182 MHz LO output frequency is used as a swept reference to derive the 719 MHz frequency. The VCO is controlled so that the third harmonic of its output frequency is a constant difference from the 2182 MHz reference. This control is accomplished by the phase lock loop. Refer to Figure 7-6 for a simplified block diagram.

In the phase lock loop, the harmonic mixer generates a frequency that is the difference between the swept 2182 MHz input reference and the third harmonic of the VCO output frequency. Ideally, this difference is 25 MHz, which in turn, is compared with the 25 MHz that is divided down from the 100 MHz oscillator output supplied from the 3rd Converter. This comparison is done by the phase/frequency detector whose output is a correction voltage that drives the VCO and shifts the oscillator frequency in the direction to hold the nominal output frequency at 719 MHz. This completes the loop that causes the VCO to track the 2182 MHz reference.

Because the 3rd harmonic of 719 MHz is locked to the 2182 MHz reference, the tuning range of the 719 MHz oscillator is only one third of the tuning range of the reference. Since the range is 4 MHz, the range of the 719 MHz oscillator is 719 ±1.33 MHz.

The 719 MHz VCO (Q2014) uses a Colpitts configuration, with a printed circuit quarter-wavelength transmission line resonator, to achieve high spectral purity and good thermal stability. Correction voltage is applied to varactor diode CR1011 (which is connected at the midpoint of the transmission line resonator) to vary the resonant frequency of the transmission line over a 1.5 MHz range. A tunable transmission line (also printed) adjacent to the printed resonator compensates for variations in component tolerances and resonator dimensions. This adjustable transmission line is cut, at factory calibration, to the correct length for proper VCO operation. A scale with minor divisions every 2 MHz is

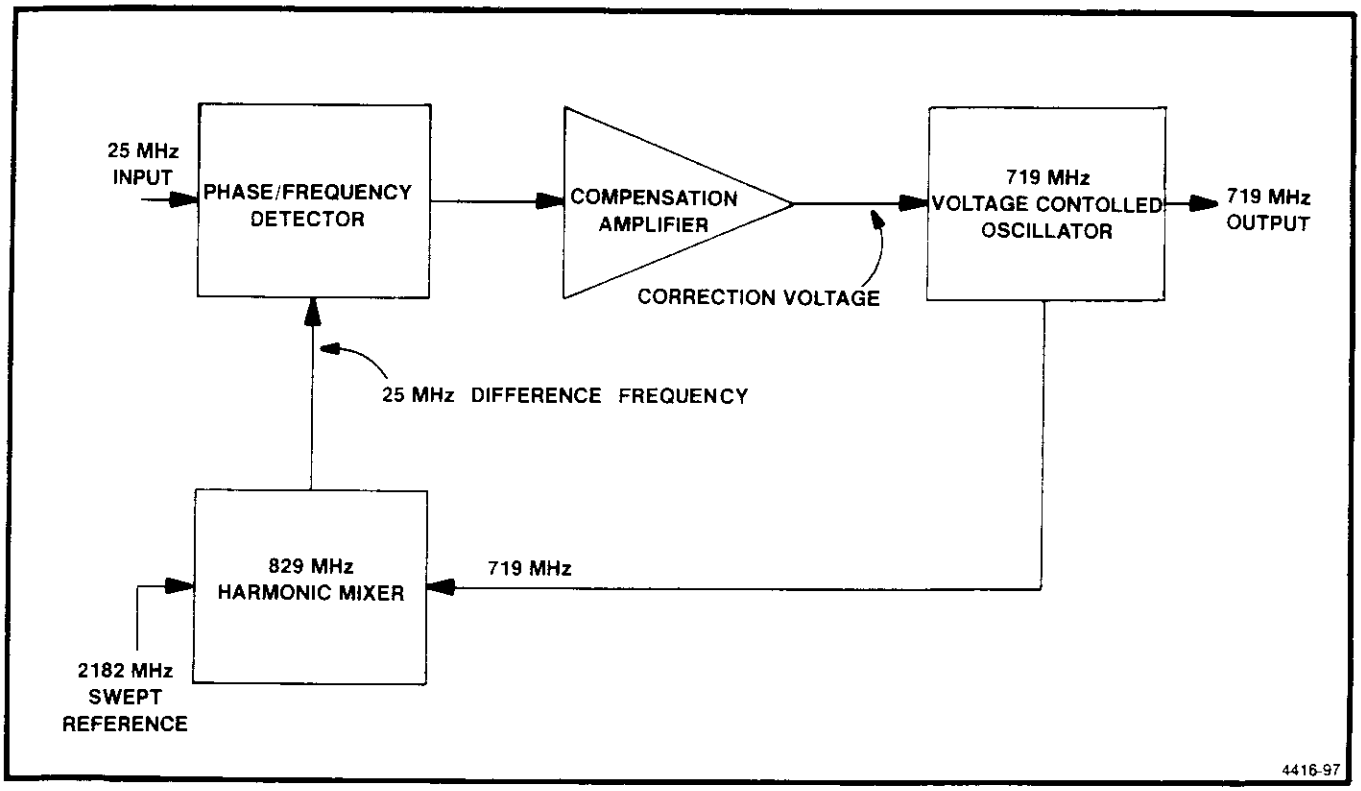


Figure 7-6. Simplified block diagram of the phase lock loop in the 829 MHz 2nd converter.

printed next to the adjustable line to aid in calibration. The output from the oscillator is extracted near one end of the quarter-wavelength line through two printed inductors and applied to output amplifiers through a power splitter.

The 719 MHz VCO is enabled or disabled, under microprocessor control, dependent upon the frequency band being analyzed, by the IF SELECT line. When this line is low, Q2017 is cut off, which turns Q2016 off. This, in turn, cuts off transistor Q3015 (which is the current source for oscillator transistor Q2014), thus disabling the 719 MHz oscillator.

From the oscillator, the +6 dBm 719 MHz output signal is applied,through a power divider consisting of resistors R1021, R1022, and R1020, to isolation amplifier Q1021. From the other side of this power divider, the signal is applied to an output amplifier (Q2021) for transmission to the 829 MHz 2nd Converter Mixer circuit. A second isolation amplifier (Q3021), identical in configuration, provides isolation between the 719 MHz oscillator output and any undesired Harmonic Mixer products.

The 829 MHz Harmonic Mixer produces not only the required 25 MHz difference frequency, but also many higher order IM products. Two of these frequencies, 744 MHz and 694 MHz, are 25 MHz from the 719 MHz oscillator frequency. The isolation amplifiers, Q1021 and Q3021, provide sufficient attenuation in the reverse direction to prevent these products from getting into the 829 MHz mixer to produce spurious signals.

To provide maximum reverse attenuation in each amplifier circuit, external RF feedback is kept to a minimum. An output matching LC network, consisting of capacitor C1025 plus a printed inductor for Q1021, and capacitor C3021 plus a printed inductor for Q3021, presents an optimum load impedance to the collector of each transistor to allow maximum power transfer to the attenuator that precedes the harmonic mixer. An input LC matching network consisting of capacitors C1023, C1022, plus a printed inductor for Q1021 and capacitors C3023, C3022, plus a printed inductor for Q3021, establishes the 50 Ω input impedance to each transistor.

A 3 dB attenuator consisting of resistors R3021, R3022, R2021, and R3023, at the output of isolation amplifier Q3021, provides a non-reflective source impedance to the mixer. Without the attenuator, mixer conversion loss could vary from unit to unit.

The 829 MHz Harmonic Mixer, consisting of diode CR2021, inductor L2014, and a half-wavelength (at 2182 MHz) transmission line, produces the difference frequency between the third harmonic of the 719 MHz oscillator frequency (nominally 2157 MHz) and the 2182 MHz reference frequency. Note that the 2182 MHz signal is supplied from the 2182 MHz 2nd Local Oscillator through coaxial connector P237 and the power divider, consisting of resistors R1021, R1023, and R1022, to a half wavelength transmission line. The VCO input to the mixer switches diode CR2021 at a 719 MHz rate. The 2182 MHz reference acts as the RF and is applied to the diode from the transmission line. The resultant 25 MHz intermediate frequency is diplexed from the mixer through the 100 MHz low-pass filter consisting of capacitor C3014 and inductor L3014. (Diode CR2021 is mounted in printed circuit board cut-outs to relieve any necessity of bending the diode leads. Lead bending may fracture the diode case.) Inductor L2014 provides a bias return path to allow the diode to switch at a 719 MHz rate.

From the 829 MHz Harmonic Mixer, the signal is applied through the above mentioned low-pass filter to cascaded amplifiers U1053 and U1044B. These amplifiers boost the −32 dBm mixer output signal to a level appropriate to drive the phase/frequency detector. IC amplifier (U1053) contains two differential amplifiers in cascade; amplifier IC U1044 contains only one differential amplifier and acts as a buffer. When the loop is first acquiring lock, such as at power-on, the nominal 25 MHz IF may be as high as 34 MHz. Two stages of amplification are necessary to ensure enough gain for the phase/frequency detector to drive the IF back to 25 MHz; the buffer is necessary to provide ECL levels to the detector.

The second input to the phase/frequency detector is the 100 MHz signal, from the reference oscillator in the 3rd Converter, via two amplifier stages, U1022A and U1022B, and a ÷4 circuit, U1036A and U1036B. The 100 MHz signal is divided down to a 25 MHz reference for application to the phase/frequency detector. Two stages of amplification are used to isolate the 100 MHz reference bus from signals generated in the local oscillator section of the 2nd Converter. This stable 25 MHz reference signal is used to lock the difference frequency from the Harmonic Mixer to 25 MHz.

The phase/frequency detector output is a voltage that is proportional to the phase difference between the 25 MHz reference and the IF signal from the 829 MHz Harmonic Mixer. This correction voltage is then applied to the 719 MHz VCO to lock it to the reference.

The detector circuit consists of two D-type flip-flops, U2047A and U2047B, and a differential amplifier stage used as a NAND-gate (U1044A). The 25 MHz reference signal, from the frequency divider, is applied to the clock input of flip-flop U2047A; the nominal 25 MHz signal from the 829 MHz Harmonic Mixer is applied to the clock input of flip-flop U2047B. The rising edge of the input signal to each flip-

flop causes the Q(bar) outputs to return to the low level only after both flip-flops have been clocked.

If the frequency out of the 829 MHz Harmonic Mixer is below 25 MHz, or if its phase lags that of the 25 MHz reference, the $\overline{Q}$ output of flip-flop U2047A will remain high longer than the $\overline{Q}$ output of U2047B. If the frequency out of the Harmonic Mixer is above 25 MHz, or if its phase leads, the opposite will occur. When the two flip-flops are clocked at the same frequency and phase, the two outputs will be high for the same amount of time. The $\overline{Q}$ outputs are applied to a compensation or differential amplifier U3053,that determines which output is high for the longer time.

Compensation amplifier U3053 provides part of the loop gain to ensure that the 719 MHz oscillator will track the sweep of the 2182 MHz reference oscillator. The compensation amplifier also limits the loop bandwidth to 100 kHz to make certain that the loop will not oscillate. Note the differential inputs to the amplifier each include a low-pass RC filter to attenuate the undesired high frequency clock pulses from the phase/frequency detector.

The nominal swing of the U3053 output is from +12 to −12 V. Since the compensation amplifier is capable of considerably more output than is needed to control the oscillator, a voltage divider is used to limit the output and reduce amplifier related noise. This voltage divider, consisting of resistors R2053, R2054, R3051, and R3052, reduces the possible ±12 V swing to +5 V to +12 V, as required by varactor diode CR1011. Nominal voltage swing in a locked condition is +6.75 to +7.5 V. Thus, dependent upon whether the Harmonic Mixer frequency is above or below 25 MHz, the correction voltage swing, applied to diode CR1011, is more than nominal to correct the oscillator frequency.

Front Panel 2nd Local Oscillator Output Circuit

A portion of each 2nd LO output signal is sent to the front panel 2nd LO OUT connector. This output provides signal for external accessory equipment, such as a tracking generator. Each local oscillator (719 MHz and 2182 MHz) output is applied through power dividers to a power combiner for application to the 2nd LO OUT connector.

The 719 MHz oscillator frequency is applied from a power splitter (R3027, R3028, R3029) through a 1 GHz low-pass filter (C3025,C2024, C1023, C1021, and three printed inductors), to the power combiner (R2024, R2025, R2026), and the front panel 2nd LO OUTPUT. The 2182 MHz oscillator signal is applied through a power splitter (R1021, R1022, R1023), a 2.2 GHz band-pass filter (consisting of coupled quarter wavelength printed lines) to the power divider (R2024, R2025, R2026) and the front panel 2nd LO OUTPUT.

Both 2nd local oscillator signals, 2182 MHz and 719 MHz, are present at the front panel when the 829 MHz 2nd Converter is selected.

719 MHz Output Circuit

The 719 MHz 2nd Local Oscillator signal is applied is applied through divider resistors R2021, R2023, and R2024 to isolation amplifier Q2021. Q2021 boosts the signal level from about 0 dBm to +12 dBm to drive the 829 MHz mixer. The output of the amplifier includes a 3 dB attenuator (consisting of resistors R2027, R2028, and R2029), to ensure a 50 Ω non-reflective source impedance. The signal level at test point J2026 is typically −6 dBm.

110 MHz IF AMPLIFIER, 3RD CONVERTER, 100 MHz REFERENCE, AND REFERENCE LOCK ◇4◇ ◇17◇ ◇18◇

The 110 MHz IF Amplifier and 3rd Converter down converts the 110 MHz output signal from the 2nd Converter to 10 MHz for the Variable Resolution circuits. A 100 MHz crystal controlled local oscillator is phase locked to either a precise internal 10 MHz reference or an external 1, 2, 5,or 10 MHz reference. This 100 MHz is applied to the mixer and, through output amplifiers, to many other circuits throughout the instrument as a reference signal. It is also available for external use at the front-panel CAL OUT connector.

The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section band-pass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the band-pass filter, the signal is applied to the converter, which consists of a mixer, an oscillator, and various output amplifiers.

110 MHz IF AMPLIFIER ◇17◇

Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for conversion losses in the three mixers. Typical gain for the amplifier is 21 dB. The amplifier consists of three stages of amplification and an attenuator. The first two mixers in the RF system offer no high-frequency gain; therefore, it is important that this amplifier exhibit low noise characteristics. It must also be relatively free from third-order intermodulation distortion.

Signal input is applied through an impedance matching band-pass filter (L2044 and C325) to a parallel tuned circuit. The signal is injected into the parallel-tuned circuit through a tap in the inductor and taken out at the high impedance side through variable capacitor C2047. Inductive input provides for conversion to high impedance within the tuned circuit; the extra capacitor on the output provides for conversion back to 50 Ω nominal. The primary tuning capacitor, C325, adjusts the resonant point; the output capacitor, C2047, is adjusted in combination with C325 for good impedance match at 110 MHz. This is done with a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, which is the first stage of amplification. This is a broad-band feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054), not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged "T" adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes, CR3030 and CR1029, in the mode when the resistance to RF signal flow is controlled by the current through the diodes. Refer to Figure 7-7 to aid in understanding the following description.

If resistor R1 in Figure 7-7 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, to produce infinite signal attenuation. If resistor R1 were set to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, to produce almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

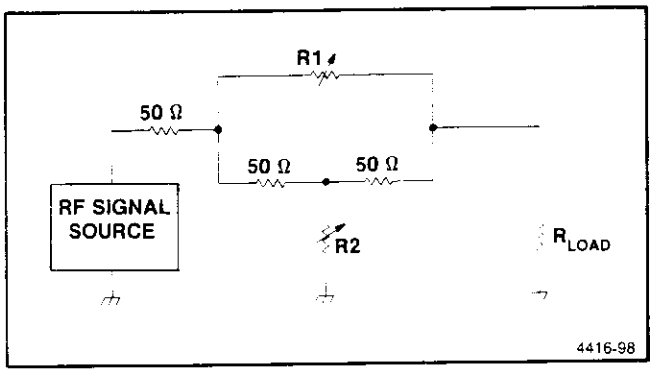


Figure 7-7. Bridged "T" attenuator equivalent circuit.

Resistors R3035 and R2030 on the 110 MHz Amplifier board, A32A1, establish a constant current of approximately 2 mA from the 15 V supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 V supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, which results in a good impedance match over a broad range. The RF signal path is determined by the exact amount of current through CR3030; part of the RF signal path is through CR3030 to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broad-band feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a resonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

With Gain potentiometer R1015 set for maximum gain (least attenuation), the gain of the 110 MHz IF Amplifier is approximately 26 dB to 27 dB. R1015 is normally adjusted for total gain of 21 dB.

The output signal from the 110 MHz IF Amplifier is applied through the 110 MHz band-pass filter, FL36, to the 3rd Converter.

110 MHz BAND-PASS FILTER

The 110 MHz band-pass filter is a three-section filter using helical resonators, which determine the widest resolution bandwidth of the analyzer. The filter provides image rejection to prevent the mixer from producing 10 MHz outputs from input signals of 90 MHz, and it also limits the noise spectrum that appears at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small encapsulated helical resonators that are tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 pF capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed by setting the three trimmer capacitors. Insertion loss is approximately 4 dB to 4.5 dB. From the filter, the 110 MHz signal is applied to the 3rd Converter.

3rd CONVERTER ④

The 3rd Converter consists of a crystal and phase locked 100 MHz oscillator and mixer. It outputs the 3rd IF of 10 MHz, for the VR, and a stable 100 MHz reference for other circuits within the instrument.

100 MHz Oscillator ⑰

A Colpitts oscillator is formed by Q2038, L1041, C1038, and related components. Y3038 is a 100 MHz crystal that operates in a series resonant mode in the feedback loop of the oscillator. L3041, varactor diode CR3039, and Y3038 form a series resonator that is used to tune the oscillator approximately ±1 kHz (the voltage on CR3039 is varied, which changes its capacitance). RPL GND is tied to ground in the Reference Lock module. RPL VOLTS TUNE varies from 0 V to +12 V to tune the oscillator to exactly 100 MHz. P2042 shorts across the tune circuit for adjustment purposes. The output of the oscillator is coupled through C2042 to differential amplifier Q2042/Q2041. The two separate outputs of approximately 2 V peak-to-peak amplitude go to three hybrids (mixer U3051, distribution amplifier U3031, and calibrator U2022) on the 3rd Convertor board.

Mixer

At mixer U3051, 100 MHz enters on pin 2 and is amplified to drive a ring diode mixer. 110 MHz enters on pin 10 and is mixed with the 100 MHz to yield mixing products at 10 MHz and 90 MHz. The 10 MHz signal passes through a low-pass filter and is sent to the Variable Resolution Input circuit, while the unwanted 90 MHz signal is terminated in a 50 Ω resistance within the mixer.

Distribution Amplifier

U3031 distributes a 100 MHz signal to other modules in the instrument. The input level on pin 2 is typically 2 V peak-to-peak, while the output level is 0 dBm into a 50 Ω load.

Calibrator

U2022 and related components regulate a 100 MHz signal to −20 dBm for the front-panel CAL OUT connector, through coaxial connector J1011. VR1051 serves as an accurate 6.2 V reference, which is attenuated to approximately 1.2 V and applied to pin 6 of U2022. The 100 MHz signal enters pin 1 and passes through a variable attenuator pin diode. The signal is then amplified and passed through a low-pass filter to remove any harmonics. The signal then enters a peak detector and comparator where the peak amplitude of the 100 MHz signalis compared to the 1.2 V reference on pin 6. An operational amplifier then adjusts the attenuation level of the pin diode to maintain a constant signal level. The output of this operational amplifier can be measured on TP3011. A small portion of the 100 MHz signal is attenuated through R2011 to −20 dBm. R1021 and R1022 supply bias current to the peak detector circuits. The voltage on pins 7 and 8 should typically be +5 V.

C2023, C2011, and related components form a high-pass filter to allow harmonics of 100 MHz to pass through to the front panel. The final result is a calibrator signal rich in harmonics with an accurate 100 MHz amplitude.

REFERENCE LOCK 18

The Reference Lock module consists of a reference detector, frequency synchronizer, phase/frequency detector, and tune window detector. Either an internal 10 MHz reference or an external 1, 2, 5,or 10 MHz reference frequency is routed through the reference detector to the frequency synchronizer. The local oscillator's 100 MHz output is divided by 100 and applied to one input of a phase/frequency detector which compares it with the 1 MHz reference frequency. The resultant error signal is amplified by the tune amplifier and applied, as a corrective voltage, to the voltage controlled 3rd LO.

External Reference Detector

Buffer amplifier Q2014 converts External Reference signals, within the range of −15 dBm to +15 dBm, into TTL compatible level. When an external signal,within the level range, is applied, it triggers multivibrator U2046B. The output of U2046B enables external signal control NAND gate U2032D, and disables the internal signal control gate U2032A. It also disables the internal 10 MHz reference oscillator by turning Q1031 on, which biases Q1033 off, and removes the +5 V supply for the oscillator. The $\overline{Q}$ output of U2046B is sent to the processor, on the EXT REF line, to indicate that an external reference frequency is in use. The microprocessor can also pull the INTERNAL SHUT-DOWN line down, during a diagnostic test, to turn the Internal Reference Oscillator off and check for loop unlock. U2032B is a wired-OR gate that gates, either, the 10 MHz from the internal gate U2032A, or the external reference from U2032D, to the frequency synchronizer U2046A.

Frequency Synchronizer

Multivibrator U2046A, synchronizes it's 1 MHz output with any of the 1 MHz multiple input signals by edge-triggering the time-out period. The 1 MHz output frequency is set by the timing components R2039,C2038, and adjustment R2042. With a 10 MHz signal applied to U2046A, adjustment R2042 is set for a 1 μs period, with 65 ns between the falling edge on TP2046 and the next falling edge on TP1044.

Phase/Frequency Detector

The 100 MHz, from the 3rd Local Oscillator, is divided by 100 and converted to a TTL level by prescaler U2020. The 1 MHz from U2020, is fed to the clock input of D-type flip-flop U1044A. The 1 MHz from U2046A, is applied to the clock input of D-type flip-flop U1044B. The two flip-flops and NAND gate U2032C, form the Phase/Frequency Detector. R1034, R1035, and C1037, along with it's counterpart, on the output of U1044A,form a low-pass averaging filter for the outputs of the flip-flops. When the two input frequencies are equal and in phase, the composite output of the averaging filter is +2.5 Vdc.

Tune Amplifier

The FET input operational amplifier (U1034) takes the output of the phase/frequency detector, amplifies the error and supplies an appropriate tune voltage to the 100 MHz voltage controlled oscillator. The tune amplifier, with feedback components C1031, C1038, R1028, and R1029, determine the loop transfer characteristics. The loop dc gain is very high which takes advantage of the high accuracy of the internal or external references. The loop ac gain (determined by C1031) rolls off very quickly so any phase noise, on an external reference signal, is not amplified.

Lock Detector

U1012 is used as a tune volts window detector. R1013, R1012, and R1011 set the upper threshold at 11 Vdc, and the lower threshold at 2 Vdc. As long as the tune volts stays within these limits, a high output tells the processor that the 3rd LO loop is locked. A low output from U1012, indicates that the reference oscillator frequency is beyond the 3rd LO's tune range. This REF LOCK status line, along with the other two processor interface lines, is routed through the Sweep board for processor interrupt generation.The processor reads the lines and displays their status on the crt readout.

IF SECTION ◇5◇ ◇19◇ ◇20◇ ◇21◇

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution through selective filtering, levels the gain for all bands, and logarithmically amplifies and detects the signal to produce the video output to the Display section.

System bandwidth resolution is selectable, under microcomputer control, from 1 MHz to 100 Hz in decade steps plus 30 Hz.This selection is performed by the Variable Resolution circuits. Two sets of filters are used to establish the bandwidth. Band-pass filters are also included at the circuits input and output.

Significant gain is also provided by several stages of amplification within the Variable Resolution circuit block. Other gain steps, under microcomputer control, are also provided by switching gain blocks in or out of the signal path. These gain blocks when switched in combination, provide −10, +20, or +30 dB of additional gain.

Leveling, to compensate for front-end losses, is also included in the Variable Resolution circuit block. Because there are greater front-end losses in the higher frequency bands, band leveling amplification is required for these bands.

To calibrate the graticule in dB/division, a logarithmic amplification of the signal is required. This is performed by a seven stage amplifier that produces an output proportional to the logarithm of the input; thus, the screen displacement can be selectable as to amount of change per division, and can be proportional to the input level change. For example, in the 10 dB/div display mode, each division of displacement on the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

An area detector follows the logarithmic amplifier to produce a positive- going output signal that is applied to the display section as the VIDEO signal.

Variable Resolution Circuits ◇19◇ ◇20◇ ◇21◇

The Variable Resolution (VR) circuits establish the resolution bandwidth, under microcomputer control, and provides approximately 41 dB of system gain in band 1. The assembly consists of two sets of filters plus gain stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input requires +6 dBm for full screen, the VR circuits must provide the gain difference. (In the 494/494P the VR supplies 30 dB of additional gain and 10 dB of gain reduction for all vertical display modes as well as 30 dB of additional gain for band leveling.)

Physically, the VR section consists of two sub-assemblies that plug onto the analyzer Mother board. The input circuits are in one sub-assembly and the output section and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer VR Mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the VR Mother board. All signal interconnection is via coaxial cable.

VR Input Circuit ◇19◇

The VR Input circuit receives the 35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter, which augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026, Input Align.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased at a relatively substantial output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

A 6 dB attenuator at the output of amplifier Q1023 provides a clean 50 Ω output to the 1st Filter Select circuit and reflects a 50 Ω termination back through the amplifier for proper termination of the 1.2 MHz band-pass filter. The output signal is transmitted via jumper B.

1st Filter Select Circuit ◇19◇

The 1st Filter Select circuit operates in conjunction with the 2nd Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under the analyzer microcomputer control. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035 (it provides a low signal on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps plus 30 Hz.The data bits select a filter bandwidth according to Table 7-3.

Table 7-3
BANDWIDTH SELECTION

DB0	DB1	DB2	Bandwidth
1	0	0	1 MHz
0	1	0	100 kHz
1	1	0	10 kHz
0	0	1	1 kHz
1	0	1	100 Hz
0	1	1	30 Hz

Filter selection is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the description for the 100 kHz filter selection is applicable to all filters with the appropriate component designators.

With a content of 010 for the three data bits, line 2 from U4035 will be low. This turns on transistors Q3019 and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012. The voltage drop across R3014 and R4012 is sufficient to turn CR3010 on and reverse-bias CR3012. The same operational situation exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward-bias CR3061 and reverse-bias CR3060.

Thus the signal from the input circuit, via jumper B, is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 13 dB, with slight variations among the filters. The output level is nominally −32 dBm.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pulled toward −15 V by pulldown resistors, which forward-bias the shunt diodes (input: CR3014, CR3012, CR2013, CR2011, CR1013, and CR1011; output: CR3062, CR3060, CR2066, CR2055, CR1055, and CR4065). Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) back-bias the series diodes (input: CR3011, CR3010, CR2012, CR2010, and CR1010; output: CR4068, CR2062, CR2059, CR1059, and CR4064).

Design of the filter for each bandwidth is determined by the requirements of each band and ranges in complexity from no filter to an electronically switched dual-bandwidth filter, for the 100 Hz/30 Hz resolutions.

A filter is not used in the 1 MHz section, because this circuit section is preceded by two filters that accomplish the required function; the first is the 1 MHz filter between the 2nd and 3rd Converters, the second is the 1.2 MHz filter in the input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for the loss when a filter is used.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C3023 and C3035 provide for input and output adjustments. Impedance matching is accomplished at both input and output by series capacitors C3020 and C3048, respectively.

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator consisting of R2027, R2026, and R2028 is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 Ω impedance with broadband transformers T2035 and T2055. A 2 dB attenuator consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz/30 Hz filter is an electronically switched filter that has a bandwidth of 100 Hz when its input and output ports are low (−15 V) and 30 Hz when high (+15 V dc). When 100 Hz is selected, output 5 (pin 6) of decoder U4035, outputs a low. This low turns transistor Q1020 on which forward biases CR1010 and back biases CR1011. This applies the IF to the input of the 100 Hz/30 Hz filter FL690. At the same time Q4050 is turned on which applies forward bias to CR4064 and back bias on CR4065. The output of FL690 is now connected to the input of the 10 dB Gain Step board through pin K.

When output 6 (pin 7) of decoder U4035 is high,Q1019 and Q1055 are off. This applies −15 V to the input and output ports of the 100 Hz/30 Hz filter FL690 so it is in the 100 Hz mode. When output 6 of U4035 is low, Q1019 and Q1020 are on as well as Q1055 and Q4050. This provides forward bias for CR1010 and CR4064. At the same time

Q1019 and Q1055 are turned off which applies +15 V to the input and output ports of FL690 switching it to its 30 Hz mode.

Diodes CR1017, CR1021 and CR1018, CR1022 provide limiter and clamping action at the filter input to remove RF excursions when the dc potential at the filter input and output switches.

10 dB Gain Steps Circuit ⑲

The 10 dB Gain Steps circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification; one stage provides variable gain and the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is −25 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T4019, to the first amplifier stage consisting of a differential pair, Q3016 and Q2027, and an emitter follower output amplifier, Q1036. Negative feedback through R1031 and R2051 provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 Ω.

Gain of the input stage is fixed for all resolution bandwidths except 30 Hz. The gain for 30 Hz resolution is set to a precise level by activating Q2015. Transistor Q2015 is turned on when pin L goes low. This adds R2025 (30 Hz Level) across feedback resistor R2051. Adjustment R2025 can now set the gain of the stage.)

The output from the 1st stage is then applied to a common emitter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from Q4035 on the VR #1 Mother board, A69A1, the transistor saturates and shunts the emitter load resistor R3048 with R3038 and 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front-panel AMPL CAL adjustment. Gain range is approximately 14 dB.

Output impedance of the stage is 50 Ω, set by resistor R1064. Nominal output level is −2 dBm for a full screen display. This level may be as high as +8 dBm when MIN NOISE is active. A 10 dB gain is removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps Circuit ⑳

The 20 dB Gain Steps circuit provides −6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal −2 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common emitter amplifiers, each using emitter degeneration. A change of the emitter resistance is used to change the amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is −10 dB, with Q2018, Q2042, and Q1062 biased off. This provides a nominal −12 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

Q2018 and Q2042 are turned on, when pin V is low, increasing the total gain of the first two amplifiers 20 dB. Poteniomenter R2023 (20 dB Gain) is used to adjust the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at −10 dB. This adjustment allows the gain shift to be set exactly to +20 dB.

When pin Y is low, Q1062 is saturated. This raises the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R2060 allows the gain shift to be set exactly to +10 dB.

Gain of the 20 dB and 10 dB gain step circuits is controlled by data bits 0, 1, and 2. Data is latched on the output of decoder U3017, on the VR #2 Mother board and when the bits are high, turns on transistor Q4035, Q3035, and Q4037. The resultant low out, turns on the respective gain step circuit. Table 7-4 shows the state of bits 2, 1, and 0 and the gain shifts of amplifier stages Q2043, Q1025 plus Q1035, and Q1043.

The output signal from the 20 dB Gain Steps circuit is applied through an interconnect coaxial cable to the VR Band Leveling circuit.

Band Leveling Circuit ⑳

The two amplifiers,in the Variable Resolution Band Leveling circuit, correct gain variations through the front end. These band-to-band variations are due to the different modulation products out of the 1st Converter and losses through the Preselector.

Table 7-4
GAIN STEP COMBINATIONS

Required Gain Addition	Data Bits			10 dB Gain Step Circuit		20 dB Gain Step Circuit			
	2	1	1	Q2043	Pin N	Q1025+Q1035	Pin V	Q1043	Pin Y
10 dB	0	0	1	10 dB	0	0 dB	1	0 dB	1
20 dB	1	0	0	0 dB	1	20 dB	0	0 dB	1
30 dB	1	0	1	10 dB	0	20 dB	0	0 dB	1
40 dB	1	1	1	10 dB	0	20 dB	0	10 dB	0

Nominal signal input level for band 1 at 100 kHz resolution, in the Min Distortion mode, is −12 dBm. This decreases some for the higher bands. The output level is about −2 dBm . This output level is kept constant by using the microcomputer to adjust the amplification through this circuit for each band.

The two amplifier stages on this board are similar to the 10 dB gain steps circuits. A stage consists of a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

The first stage (Q2015, Q2019, and Q1025) has a gain range of 13.5 dB by controlling the bias of PIN diode CR2021 in the feedback loop. Bias for this diode depends on a voltage divider network consisting of an array of variable resistors on the VR #2, Mother board A68A1 with the divider network selected by the microcomputer.

The second stage (Q1031, Q1033, and Q1041) is similar, except the gain change is a one step change of approximately 12.5 dB. This gain step occurs in the higher bands (4 through 11). If required, gain change is activated by the microcomputer through user-selected diodes and transistor Q2046.

The 494/494P is normally calibrated with the band 1 gain control resistor set for minimum gain. Gain is then added as required for the higher bands. Data bits 3 through 6 select gain for each band selection.

The output from this board is applied through connector EE to the 2nd Filter Select circuit.

Digital Control Circuits 

The digital control circuits, on the VR #2, Mother board provide address and data decoding for resolution bandwidth, gain step selection, and band identification for the band leveling control.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022. Data bit 7 is applied to the select input A, of the decoder, as a supplemental address bit. This bit is used to select either an address to latch data for the resolution bandwidth selection or an address to latch data for band identification and gain step selection.

Data from the analyzer data bus is applied to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection.

Data that selects gain steps and identifies the selected frequency band for control of the band leveling function is latched on the output of U3017. Output on pins 2, 5, and 6 of U3017 (corresponding to data bits 0, 1, and 2) are applied through transistors Q4035, Q3035, and Q4037, respectively, to the gain switching circuits in the 10 dB and 20 dB Gain Step circuits.

The output on pins 15, 16, 19, and 12 of U3017 (corresponding to data bits 3, 4, 5, and 6) are applied to band decoder U3023, an open collector decoder. If band 1 is selected, pin 1 of U3023 goes low and if band 2 is selected pin 2 goes low, etc. This output in conjunction with a 7.5 V reference source (provided by operational amplifier U3038B and driver transistor Q3036) produces a voltage at the output of a operational amplifier, U3038A. This voltage is indicative of the gain that must be set for each band so the level remains constant at the output for all bands.

The output of U3038A is applied through edge connector pin BB to the gain control PIN diode in the Band Leveling circuit. For example: when band 1 is selected (U3023 pin 1 low), current through Band 1 Gain potentiometer, R2031,and the emitter of Q3036 sets the voltage through R2033 to the summing input of operational amplifier U3038A. The increased output of U3038A increases the current through band leveling PIN diode CR2021 and increases the gain of the stage according to the setting of Band 1 Gain potentiometer R2031. In similar fashion, the other potentiometers (R3034, R3030, R3019, R3022, R3024, R3026, R3032, R3029, and R3028) allow adjustment of the current for each of the other bands.

An additional diode may be added to each decoder output, for bands 4 through 10, to transmit the low, via edge connector pin DD, to the gain control transistor, in the Band Leveling circuit, and increase the gain more for these bands. These diodes are CR3022, CR3023, CR3024, CR3025, CR3031, CR3027, and CR3026. If needed these diodes are installed during instrument calibration.

+5 V Regulator Circuit 

The +5 V regulator circuit, U3041, supplies a noise-free −5 V source for the VR system. This is required because of noise in the +5 V main supply.

2nd Filter Select Circuits 

Circuits on the 2nd Filter Select board operate in conjunction with the circuits on the 1st Filter Select board to set the overall system bandwidth. Banks of filters are selected under the master microcomputer control. Data bits 0, 1, and 2, from the data bus, are applied to decimal decoder U3070 (which outputs a low on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps and 30 Hz.

Filter bandwidth selection is shown in Table 7-3. Filter selection is accomplished as previously described for the 1st Filter Select circuit except the 100 Hz and 30 Hz filter.

When 100 Hz resolution is selected, pin 6 (output 4) of U3070 is low. Diode CR3068 turns on and pulls line 5 low. Q2020 turns on to enable the 100 Hz/30 Hz path through CR1017. Q3013 is also biased on and shunts R3013 to ground through C4014. When 30 Hz resolution is selected, pin 7 (output 6) is low. Q2020 is again biased on to enable the 100 Hz/30 Hz path. Q3013 is biased off and R3013 is now part of the attenuator network at the input side to the crystal filter FL6015. This decreases the amount of attenuation and offsets or compensates for signal loss when in 30 Hz resolution.

The input signal, from the Band Leveling circuit via jumper EE, is routed through the selected filter to the Post VR Amplifier circuit, via jumper JJ. Nominal loss through the filter circuit is approximately 13 dB, with internal adjustment compensation for variations between the filters.The output level is nominally −14 dBm.

The filter for each bandwidth ranges from no filter at all to a temperature compensated crystal filter. An important difference between the 1st and 2nd filter select circuits is the addition of a gain adjustment in all except the 100 kHz circuit. This adjusts the amount of attenuation through the other filters and matches the output level to that of the 100 kHz filter. Since the Band Leveling circuit furnishes compensation gain to obtain equal signal levels for all bands, this adjustment compensates for variations between the filters.

No filter is used in the 1 MHz path because of the 1 MHz band-pass filter (FL 36) between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input stage. An adjustable attenuator, adjusted by R1065, is used to provide initial signal leveling to compensate or offset the gain loss associated with the other filters in the resolution circuits.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C2050 and C5055 provide for filter tuning. A 6 dB attenuator (resistors R2048, R2047, and R2049) is included at the filter input. This attenuator and the filter form a reference to which the levels of the other circuits are adjusted. Impedance matching is accomplished at both input and output by series capacitors C1047 and C6052, respectively

The 10 kHz filter uses a two-pole monolithic crystal f . The impedances at the input and output are matche) 50 Ω by T5047 and T7050. An attenuator that contains n adjustment R3039 is included at the filter input for filter variation compensation.

The 1 kHz filter is also a two-pole monolithic crystal with impedance matching transformers T4044 and T7043. A Gain adjustment is also part of the attenuator.

The 100 Hz/30 Hz filter is a compensated high-Q crystal filter. An attenuator that contains the gain adjustment is included at the filter input for filter variation compensation. A Freq Adjust, R4025 in a voltage divider circuit, calibrates the center frequency of the crystal filter.

Post VR Amplifier Circuit ◈21

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required +6 dBm output level, and provides the final band-pass filtering. The circuit consists of two stages of gain followed by a filter.

The input signal, at a nominal −14 dBm, is applied through toroid transformer T2063 to the base of common-emitter amplifier Q2056. Gain adjustment R2038, in the emitter circuit, sets the Post VR amplifier gain. The output is transformer coupled, by T1059, to the base of feedback amplifier Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback helps to provide a well-defined output impedance of 50 Ω. Input impedance is a function of transformer T1059 and resistor R1058 across the primary winding.

From the final amplifier, the signal is applied through the 1.2 MHz band-pass filter comprised of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design with an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide band-pass filter, on the order of ten percent or greater, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a band-pass filter at both the input and the output, and since the input filter in the Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance. The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at +6 dBm.

LOGARITHMIC AMPLIFIER AND DETECTOR ◈23

The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits with a dynamic range to 90 dB. The signals are amplified so the output is proportional to the logarithm of the input. The output is then applied to a linear detector which outputs a video signal. By controlling the compression curve characteristics, each dB of change in the input signal level results in an equal increment of change in the output. In the 10 dB/div mode, each division of displacement on the screen represents a 10 dB change of input signal level.

Log Amplifier Circuits

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. These circuits consist of seven ac-coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −80 dBm to −79 dBm than a change from −1 dBm to 0 dBm. For a given stage of the circuit, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude increases.

Input signal levels nominally range between −84 dBm and +6 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds, in succession, back through the remaining six stages to the first. Each stage initially produced approximately 10 dB of gain. That gain was reduced to unity, so the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

As the input signal increases from −84 dBm to +6 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages.

Table 7-5
PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4
	Beyond Logging Range			
X−10 dB	0.00316	0.01	0.316	0.1
				0.216
X Level	0.01	0.316	0.1	0.316
				0.684
X+10 dB	0.0316	0.1	0.316	1.0
			0.684	0.684
X+20 dB	0.1	0.316	1.0	1.684
		0.684	0.684	0.684
X+30 dB	0.316	1.0	1.684	2.368
	0.684	0.684	0.684	0.684
X+40 dB	1.0	1.684	2.368	3.052
X+50 dB	3.16	Beyond Logging Range		

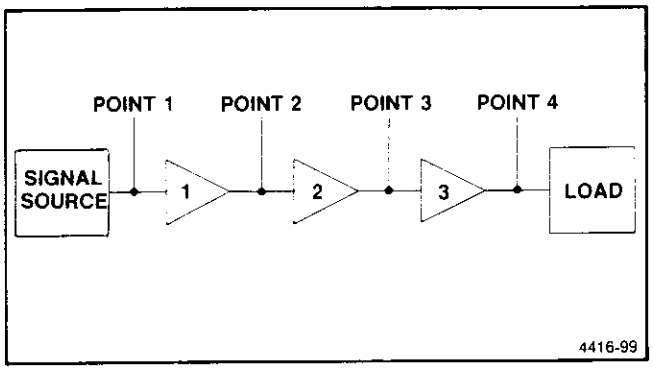


Figure 7-8. Block diagram of a three stage log amplifier.

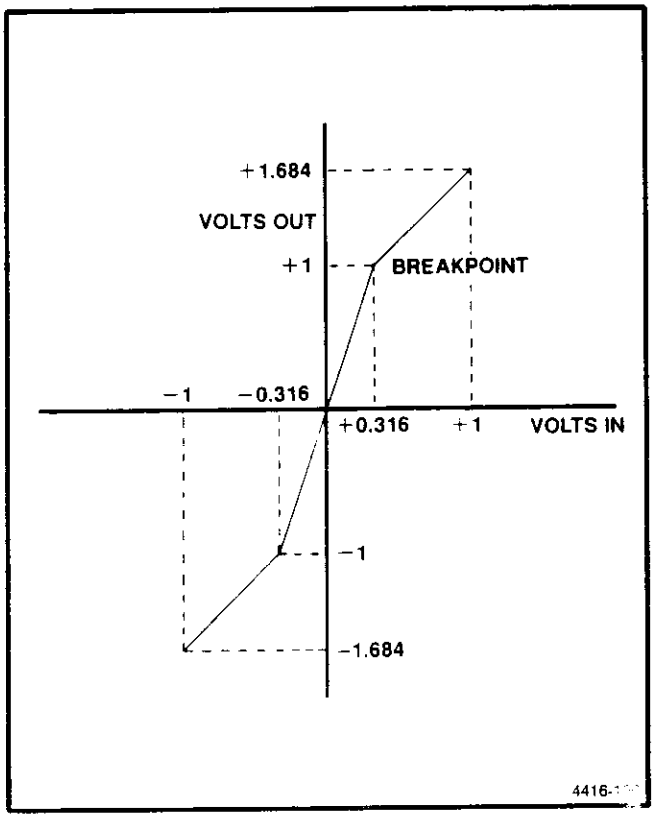


Figure 7-9. Log amplifier gain curve showing the break points.

The following description of a simple three-stage log amplifier, with one gain step in each stage, provides an aid to understanding the concept of a logarithmic amplifier. For the example amplifier described and shown in Figures 7-8, 7-9, and 7-10, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 V peak, then unity for output levels greater than 1 V peak; that is, each stage uses one breakpoint. The breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

Figure 7-8 illustrates the amplifier and the input signal source. Assume that the source has a step attenuator at the output that allows the input signal to be incremented in 10 dB steps. Table 7-5 shows the progression of gain reduction above 1 V at each amplifier stage output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 V. The gain curve for one stage is illustrated in Figure 7-9. Also note that when the level at point 1 is increased beyond 1 V, it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the nominal minimum input level, the output increment is

different. A curve of the ends of the logging range is shown in Figure 7-10.

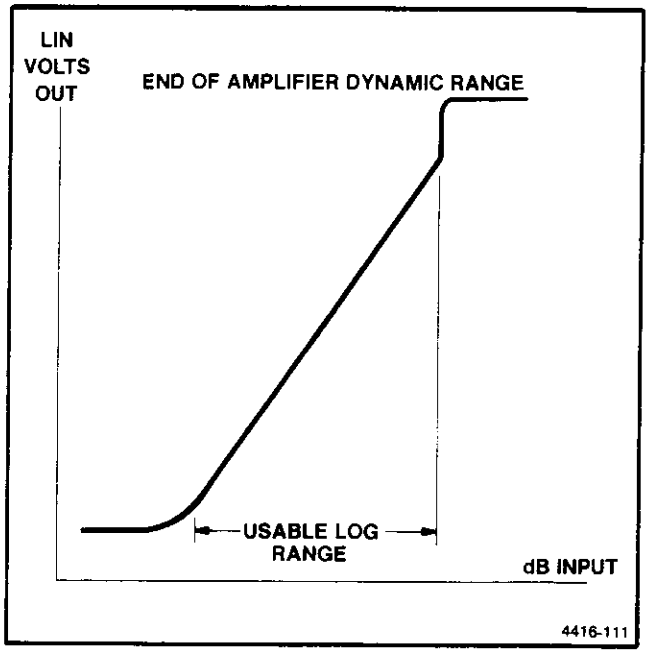


Figure 7-10. Curve showing end-of-range for a log amplifier.

The signal is applied, from the VR circuits, to input preamplifier Q3105, in the Log Amplifier circuits, through coaxial connector P621. The input preamplifier provides transfer from 50 Ω to the high-impedance input of the first amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/Q1095, Q3090/Q1080, Q3075/Q1070, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, with the exception the first three stages contain an extra set of diodes for a second gain step.

Typically, when the input level to transistor Q3015 is less than approximately 60 mV peak-to-peak, the transistor conducts enough to maintain forward bias on series limiting diodes CR4015 and CR4012. The RF signal path at that level is through both diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage, under these conditions, is approximately 10 dB. As the input signal voltage increases, more current flows through CR4015 to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and in succession, back to the first stage, Q3100/Q1095.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087 are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as previously described, with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one-two-three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector Circuit

The Detector circuit detects and filters the Log Amplifier circuit output signal and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

Although the circuit is called an operational amplifier, it is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier that consists of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes, CR5033 and CR5027, are effectively open circuited; that is, when the output is near 0 V. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the point of dc operation.

Figure 7-11 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, detector diodes CR5033 and CR5027 are used, but only the negative half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of

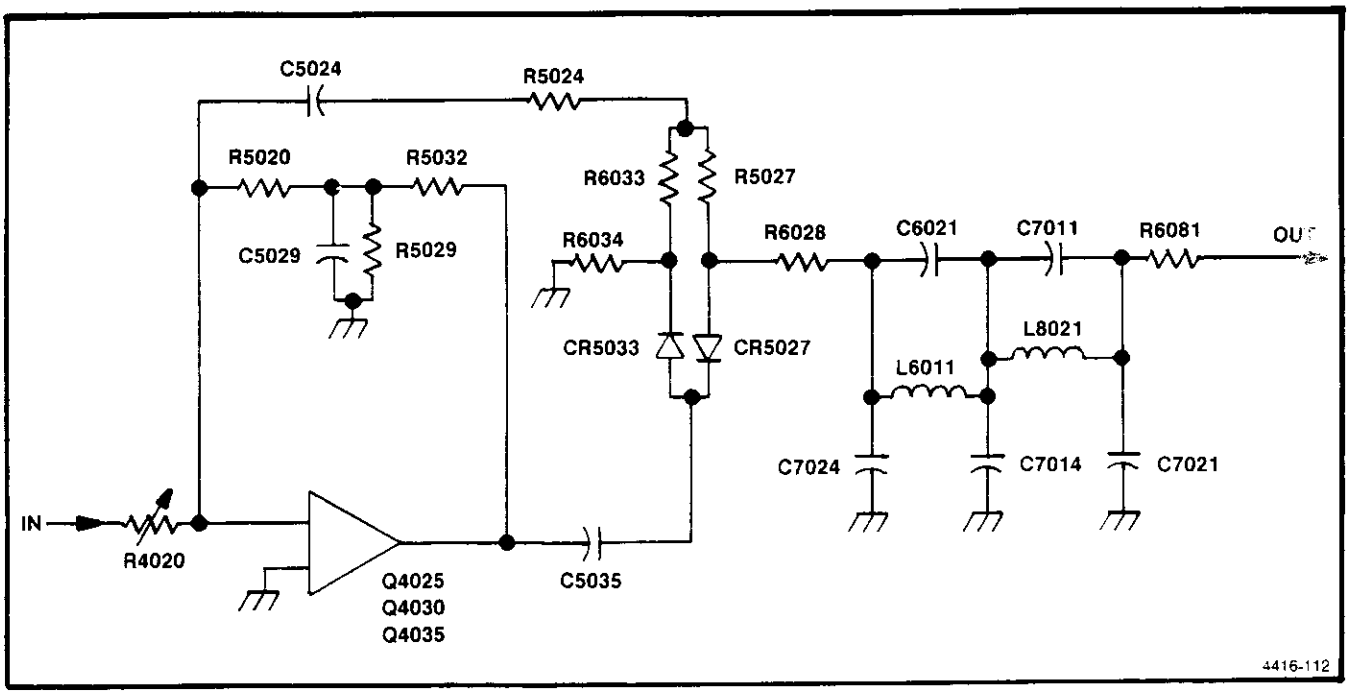


Figure 7-11. Simplified detector circuit.

the operational amplifier from affecting the detector output. This isolation occurs when the detector charges and discharges capacitors C5035 and C5024, by the current induced in each half cycle of the signal without a change to voltage level.

As shown in Diagram 22, the positive-going output signal from the detector to the Video Amplifier is applied through a low-pass filter that consists of capacitors C7024, C7014, C7021, C7011, C6021, and inductors L6011, L8021.

DISPLAY SECTION

FUNCTIONAL DESCRIPTION

The display section consists of the following major blocks:

1. The Video Amplifier processes the detected IF signal through logarithmic gain amplifiers or linear amplifiers for log or linear displays, and provides pulse stretching if selected for narrow pulsed signals.

2. The Video Processor provides band leveling to correct front-end unflatness through the bands,video filtering for noise averaging, out-of-band blanking to clamp the display to the baseline when the sweep is outside the range of the selected band, and video marker capability for use with a TV sideband adapter.

3. The Digital Storage digitizes the video and sweep signals and stores the data in memory. Stored data is then converted to analog signals for the Deflection Amplifier and Z-Axis circuits.

4. The Deflection Amplifier provides the drive voltages for the crt. This includes vertical and horizontal deflection signals as well as readout characters from the Crt Readout board.

5. The Z-Axis circuits receive and decodes data from the microcomputer; accepts control levels from the front-panel beam controls and generates unblanking signals to control the display appearance, brightness, and focus; detects power failure; monitors the instrument voltage supplies; and records the elapsed operating time.

6. The Crt Readout circuits generate the alphanumeric characters (letters and numbers) for the display.

VIDEO AMPLIFIER

Video signals, from the detector and log amplifier in the IF section, are received by the Video Amplifier. In the logarithmic mode, the signals are amplified linearly and applied to the Video Processor. In the linear mode, exponential amplification converts the logarithmic gain characteristic to linear function. In either mode, baseline compensation from the Video Processor is applied to the video signal to compensate for any unflatness in the front-end response. The pulse stretch circuit at the output of the Video Amplifier alters narrow pulses so data can be acquired and displayed by the Digital Storage logic. Signal amplitude offset circuits provide display offset for the "Identify" mode operation.

Log Mode Circuits

The log mode circuits process VIDEO signal from the Log Amplifier, and add offset for selecting that segment of the log amplifier gain curve to be displayed. The circuits also select screen display gain steps from 1 dB/div to 15 dB/div.

The VIDEO and the VIDEO 1 signals are summed at the input to operational amplifier U4090A. Front-end unflatness is compensated by the VIDEO I signals, which are equal and opposite in amplitude to the unflatness. The two signals are also summed with the reference level, set by R4071, and the output of DAC U5041.

U5041 converts the microcomputer commands to an offset signal that selects the location on the log amplifier curve for the display (see Figure 7-12).In dB/div or log display, a change in Vertical POSITION control produces an effect, after the log amplifier, that is the same as a signal level or gain change before the log amplifier. Instead of using a large amount of linear gain before the log amplifier, the output of

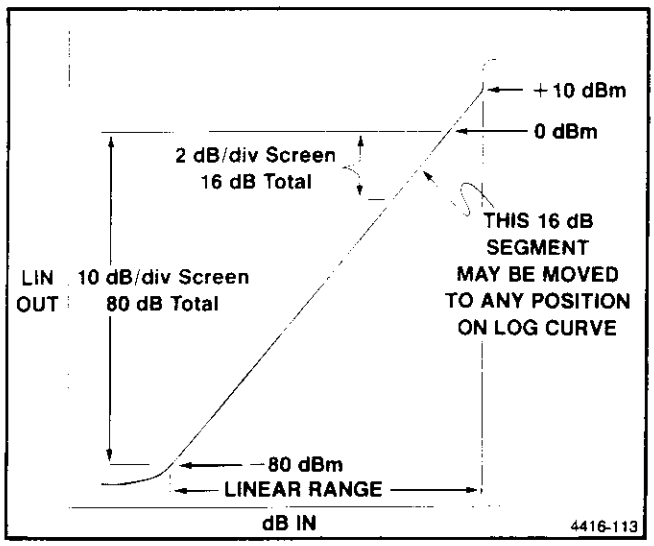


Figure 7-12. Selection of display position on the log scale.

digital-to-analog converter (U5041) effectively moves the display up or down along the log curve. This process is called "offset". Offset produces the same effect as varying the POSITION control except the display position does not change, only the signal level required to reach the reference level changes.

This process allows the linear gain to change while the top of the screen is kept constant, and it must also allow any 16 dB segment (in the 2 dB/div mode) to be displayed. Nominally, the log amplifier operates with +6 dBm at the top of the screen.

The output of U4090A is equivalent to 20 mV/dB. Full screen is 2.2 V. At 2.2 V, the output of variable log gain amplifier U4090B is 0 V. This is the only voltage at which the feedback circuit switching network resistors of preamplifier U4090B can be switched without changing the output voltage. (The switching network is described later in this discussion.) The 2.2 V output of U4090A is adjusted to full screen by Input Ref Lvl potentiometer R4071.

From U4090B, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 5 when it is high) to operational amplifier U4090C, pin 10. The signal then travels through emitter follower Q4100 to the Video Processor via the LOG CAL adjustment on the front panel. Output Ref Lvl (output reference level) potentiometer R4081, in the input circuit to U4090C, is adjusted so the output level is a full screen display after the Input Ref Lvl potentiometer R4071 is set for no change in the output of U4090B when switching between the 10 dB/div and 2 dB/div modes.

The basic adjustment sequence for the potentiometers is as follows.

1. The digital-to-analog converter output voltage is adjusted by the front-panel LOG CAL control so that the output is appropriate for 10 dB/div.

2. The Log Amplifier detector circuit Log Gain R4020, is adjusted so the Log Amplifier output agrees with the digital-to-analog converter output.

3. Input Ref Lvl potentiometer R4071 is adjusted a constant for a constant output level from U4090B, for both the 10 dB/DIV and 2 dB/DIV display modes.

4. Output Ref Lvl R4081 is then adjusted for a full screen display.

The gain switching network provides for 15 resistance values to be switched into the feedback path of variable log gain amplifier U4090B. The network consists of FET switches Q4075, Q4070, Q5070, and Q5075, and resistors R6081, R6080, R6073, and R6082. The FET switches, controlled by data bits 0, 1, 2, and 3 from the analyzer data bus, connect feedback resistors for U4090B in 15 value combinations determined by the binary content of the four data bits.

Linear Mode Circuits

The linear mode circuits accept the log preamplifier U4090A output and rescale the signal level to linear values. Since no switching is provided by the Log Amplifier circuits (i.e., all signals are logarithmically scaled), the signal level must be re-exponentiated to operate the system in the linear mode. High gain is required at the top of the screen and low gain is required at the bottom of the screen to offset the characteristics of the Log Amplifier circuits.

In addition to the signal path described for the log mode circuits, the output from preamplifier U4090A is also applied to linear mode operational amplifier U4090D, with a successive resistor network in the feedback path. From this amplifier, the output signal is applied through FET Q5095 (if that transistor has been turned on by data bit 4 from the analyzer data bus being a 1) to the summing node at the input of output amplifier U4090C. After this point, the signal path is identical to that of the log mode description.

Starting at the signal level that represents the top of the screen (0 V) at the output of linear mode amplifier U4090D, the operation of the network is as follows.

With a +6 dBm input from the Log Amplifier to the Video Amplifier, the output of U4090D is 0 V. At that level, the feedback path is only through resistor R4097. The other feedback resistors (R4096, R5103, R7092, and R5107) are not in the path, because the switch transistors are biased off by the bias network consisting of resistors R5111, R4109, R6085, R4105, and R4103, plus diode CR4103. (The diode is included for temperature compensation purposes.) As the display moves away from full screen, the output voltage of U4090D increases and turns transistor Q6115 on. This places R4096 in parallel with R4097 to reduce the gain. As the voltage output increases, transistors Q6110, Q6090, and Q6095 start to conduct in sequence, adding resistors R5103, R7092, and R5107, respectively, across the feedback path. This effectively reduces the gain of U4090D exponentially. The reaction characteristics of the transistors smooth the step transitions, to produce a smooth exponential gain curve.

Pulse Stretch Circuit

The pulse stretch circuit consists of FET switch Q7110 and the associated components in the feedback path of output operational amplifier U4090C. When the pulse stretch mode is not selected (data bit 7 on the instrument data bus is low), pin 13 of U6060 pulls down to −15 V, and Q7110 is biased off. This removes C8104 from the circuit and also supplies sufficient negative bias though R7105 to keep CR8107 forward biased. With CR8107 on, the feedback loop for U4090C, through Q4100 and R7094 is closed so the signal output will fall as fast as its rise.

When the pulse stretch mode is selected (data bit 7 going high),the open collector output of U6060 (pin 13) is allowed to float. This turns Q7110 on which completes the path for C8104 to ground. During signal rise time, C8104 now charges through the low impedance of CR8107. The feedback path for U4090C is still closed which provides a fast risetime. When the output of U4090C begins to fall, CR8107 turn off and the signal fall time is now a function of the RC time constant of R8106 and C8104, since the feedback loop for U4090C is now open. CR7103 turns on to prevent U4090C from slewing to far negative.

The identify offset circuit shifts the display when the identify feature is in operation so true and false signals can be identified. This feature is implemented elsewhere in the analyzer, except for the offset. When the "Identify" feature is in operation, it allows the operator to distinguish between responses which result from signals at the analyzer center frequency (true signals) and those that are produced by other harmonic conversions (false signals). This is accomplished by moving the 1st and 2nd LO frequency an equal and opposite amount, related to the 1st LO harmonic used, or by moving the 1st LO twice the IF divided by the harmonic number (N), on every other sweep. The result is that false signals will shift a significant amount horizontally on the display while true signals will remain within close approximation to each other. The offset circuit shifts the alternate or "Identify" sweep vertically (down approximately 2 divisions). This offset is accomplished by the microcomputer setting DB 6 high, during "Identify" sweep, so the open collector output of U6060 (pin 14) goes from −15 V to open. This removes the current normally flowing in R7097 from the summing node of U4090C and causes a −1.2 V or 2 division shift in the VIDEO 2 output level of Q4100.

Digital Control Circuit

The digital control circuit provides the control signals that select the various Video Amplifier functions. Address 78 and 79 are decoded by U6070 and sent through inverter U5070 as clock or enabling signals for gain latch U6040 and mode latch U6050.

Gain latch IC U6040 is an 8-bit latch that supplies command data to 8-bit digital-to-analog converter U5041 to offset the Log Amplifier output signal. Mode latch U6050 is an 8-bit latch that supplies command data through buffer U5060 and U6060 to select the resistors in the dB/div switching circuit and to select identify, pulse stretch, and log or linear mode.

VIDEO PROCESSOR 

The Video Processor performs four functions. The first is unflatness compensation for front-end response variations. The second is video filtering, which provides the selection of six video bandwidths (30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz) under control of the instrument microcomputer. The third function is out-of-band blanking, which blanks the upper and lower ends of the local oscillator swept frequency range to provide a selected window for the display. This function is also controlled by the microcomputer. The fourth is the capability to generate a negative-going ditch marker on the video display for interfacing with a 1405 TV Sideband Adapter.

Interface with 1405 TV Sideband Adapter

The TEKTRONIX 1405 TV Sideband Adapter is a specialized tracking generator that is used with the 494/494P to analyze the response of a television transmission system. The spectrum analyzer monitors the RF output of the transmitter while the sideband adapter drives the video input of the system. The video input may be at the transmitter site, the head end of the studio-transmitter link, or the video switcher in the studio. The sideband adapter must be connected to the 1st LO of the 494/494P by a short length of coaxial cable.

The system shown in Figure 7-13 depicts a TV transmitter operating on Channel 10 with a video carrier at 193.25 MHz. The sideband adapter is tuned to Channel 10. The spectrum analyzer is tuned to 195.25 MHz with a span setting of 1 MHz/Div (for purposes of illustration, the sweep is assumed to be halted at the center frequency of the analyzer).

The sideband adapter applies a 2 MHz signal to the AM modulator of the video transmitter. The modulator produces a lower sideband at 191.25 MHz, a carrier at 193.25 MHz, and an upper sideband at 195.25 MHz. This signal is amplified, filtered, and combined with the FM aural signal. The composite signal is sensed by a RF pickup and applied to the RF Input of the spectrum analyzer.

The 1st Converter of the spectrum analyzer applies the composite signal to the 1st mixer. The composite signal is

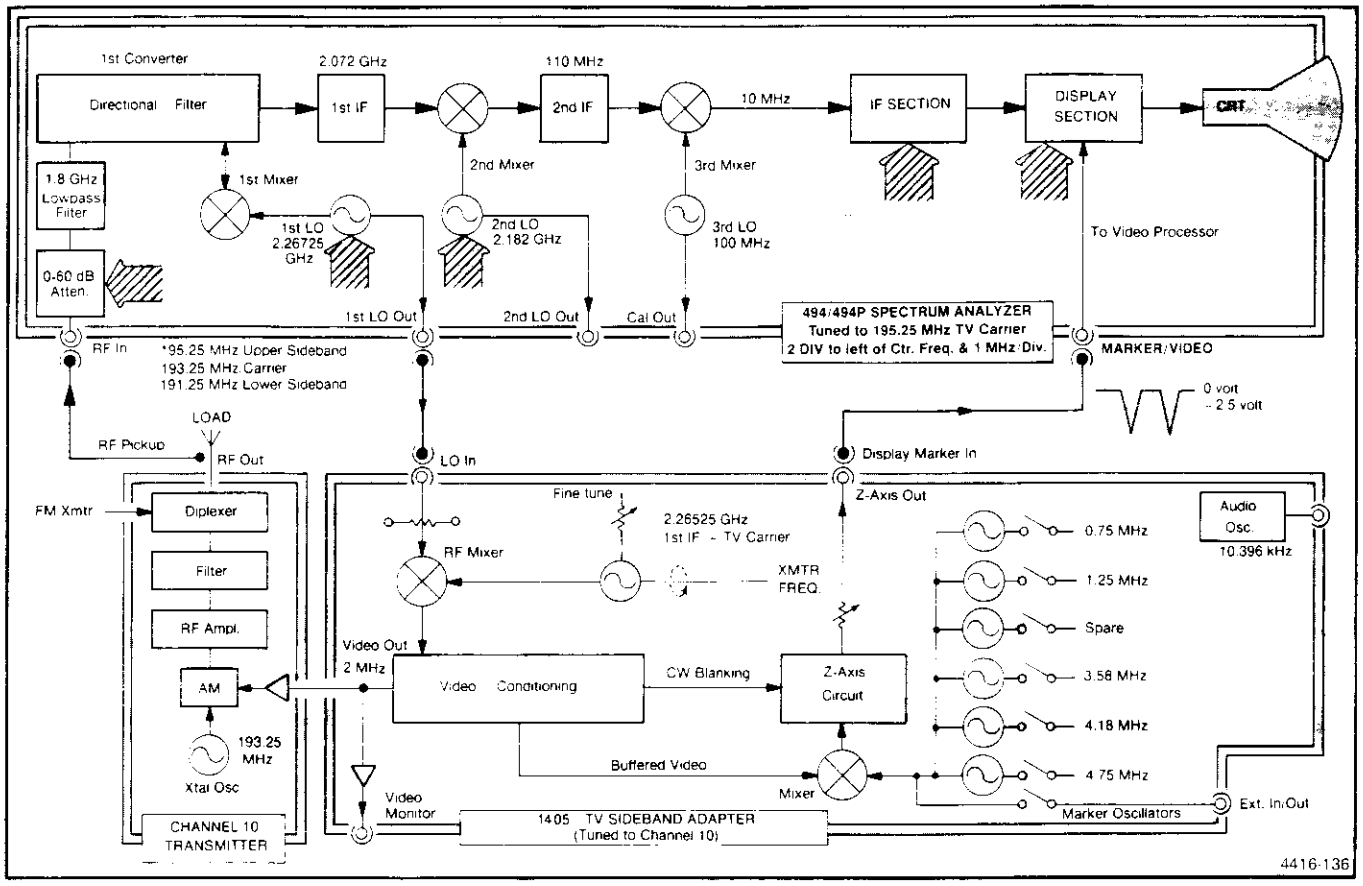


Figure 7-13. Functional diagram showing the 494/494P with the 1405 TV Sideband Adapter System.

mixed with a 2.26725 GHz signal from the 1st LO, forming three products. The subsequent stages of the analyzer accept only the 2.072 GHz product and reject the rest. For frequencies used in this example, the accepted product is the difference between the 1st LO and the upper sideband of the TV signal. The product is converted twice more, amplified, filtered, logged, and detected. This detected signal is applied either directly to the video amplifiers of the crt or to digital storage.

The spectrum analyzer 1st LO signal is applied to the RF mixer of the sideband adapter. The 2.26525 GHz signal from the tunable LO is subtracted from the 2.26725 GHz signal from the spectrum analyzer LO, yielding a 2 MHz product. This video frequency signal is conditioned with sync and blanking signals and applied to the video input of the TV transmitter.

When the 494/494P Spectrum Analyzer is sweeping, the video signal starts at 3 MHz, falls to 0 Hz, and rises up to 7 MHz. During this interval, the analyzer displays the lower sideband as it moves toward the carrier, displays the carrier, and then displays the upper sideband moving away from the carrier. Since the 494/494P and 1405 TV Sideband Adapter system is similar to a tracking generator system, it rejects noise and uncorrelated signal. This allows normal in-service use of the transmitter by adding a low level (1 to 3 IRE units) cw signal to the video or by using full levels with a VIT inserter.

The sideband adapter can insert frequency markers at preselected deviations from the carrier frequency. Six selectable crystal oscillators have their outputs mixed with video signal and applied to a Z-Axis circuit. This circuit produces two negative pulses as the video signal sweeps through the crystal oscillator frequency. These pulses are applied to the spectrum analyzer marker input, where they appear on the crt as two notches on either side of the marker frequency. The sideband adapter allows the width and depth of the notches to be adjusted with the Width and Intensity controls.

Video Marker

The Z-Axis signal from the sideband adapter is applied to the MARKER input connector on the rear panel of the 494/494P instrument. This negative-going signal is applied through the Accessories and Mother boards to the Video

Processor board. The signal is applied to the emitter of Q4060 and turns the transistor on, which pulls the VIDEO OUT line down. This produces a notch in the video signal of the display to signify the location of the marker on the display.

Video Leveling

A minor slope in frequency response, caused by the 1.86 GHz low-pass filter in the front end, is corrected with band 1 Slope adjustment R1012. When operating in band 1, contacts 6 and 7 of U3025 are closed; therefore, a portion of the PRESELECTOR DRIVE signal is applied to the VIDEO 1 output signal, providing the offset necessary to correct slope difference.

Video Leveler Circuits

Video leveling compensates for analyzer front-end microwave circuit characteristics that cause unflat response in band 4 (5.4 GHz to 18 GHz). Since band 4 is a multiplied band, any unflatness is accentuated. Leveling is accomplished through programmable perturbation of the display baseline that is opposite in direction to the flatness error. As the signal power output decreases, the baseline rises an equal amount to compensate, and as power output increases, the baseline falls an equal amount. The perturbation is produced by a normalizer integrated circuit that produces 19 evenly spaced values of the input voltage, with each value corrected to compensate for unflatness.

The PRESELECTOR DRIVE signal from the 1st LO driver circuits is applied to a translation circuit that consists of two current drivers (U3045A and half of Q3038, plus U3045B and the other half of Q3038). The PRESELECTOR DRIVE signal is directly related in amplitude to displayed analyzer frequency. The nominal +10 V to −10 V excursion voltage versus frequency curve, in maximum span, relates to the full bandwidth. This 20 V maximum excursion is scaled to a precise current (from 1 mA at +10 V to 0 current at −10 V) that is applied to the normalizer IC to generate the baseline perturbation. Actual signal scaling is done by current driver U3045A/Q3038. The output signal is applied to the normalizer SWP IN input, pin 5 of U2039. The second current driver, U3045B/Q3038, generates a 2 mA reference current for the normalizer. Horizontal Freq adjustment R1069, in the input translation circuits, shifts the 19 evenly spaced points up or down in frequency to compensate for unflatness.

Normalizer IC U2039 operates as a shaper and contains 19 bi-polar transistors that turn on and off in sequence as the current input to pin 5 decreases from 1 mA to 0. The collector of each of these IC transistors is connected to a potentiometer that allows output trimming as shown on Diagram 24. Potentiometer R1061 is active with no current, and R1013 is active at 1 mA. The trimming operation is described later.

From the normalizer, the output is applied through a jumper switch to buffer amplifier U2055B, which has a gain of five, then to offset amplifier U2055A. This amplifier has a gain of two, but its primary purpose is to offset the 0 to +5 V (normal), 0 to −5 V (invert), buffer output to the levels required by the Log Amplifier circuits. The range required by the Log Amplifier is 0 to −10 V. The output voltage is a series of linear interpolations of the voltage between adjacent trimming resistors at the outputs of the normalizer. Compensation adjustment R3030 sets correct interpolation.

Jumper plug P2060 selects the input side of buffer amplifier U2055B and proper offset voltage for U2055A. This provides the means to invert the buffer output during the instrument adjustment procedure. The adjustment procedure is described in that section of this manual.

As previously noted, only band 4 requires significant compensation. Selection of band 4 is indicated by data bit 0 switching to a 1 (see the Leveling table at the top right corner of Diagram 24). When DB0 is a 1, pins 3 and 2 of switch U2015 are connected, and the output from offset amplifier U2055A is supplied out as the VIDEO 1 signal.

Minor compensation is required for Band 1, to correct a minor slope caused by the 1.8 GHz low-pass filter and 2 GHz limiter. When pins 6 and 7 of switch U3025 are connected, the PRESELECTOR DRIVE signal is offset by R4023 and R4011 and Band Slope adjustment R1012 to provide an attenuated negative-going ramp to the VIDEO 1 output line. Switch U3025 is controlled by inverter Q4025. Q4025 is activated by data bit 6 going low. As shown in the Video Blanking table on the schematic diagram, DB 6 is 1 except when Band 1 is selected.

Video Filter Circuits

Video filtering provides selection of one of six bandwidths, under microcomputer control. As shown in the Video Filter table on Diagram 24, data bits 1 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz. Either wide or narrow-band filtering is selected at the front panel (Wide band is defined as 1/30th of the selected resolution bandwidth and narrow is defined as 1/300th of the resolution bandwidth). The microcomputer makes the selection, based on such factors as sweep rate and total dispersion. With no video filtering (all data bits are 0), the video system bandwidth is 500 kHz.

Two signal inputs (EXT MARKER/VIDEO) can be applied to the video filter circuits. The EXT VIDEO signal, from the rear-panel MARKER/VIDEO connector, is applied to pin 15 of switch U3063A through edge connector pin 53. The INTL VIDEO signal, from the Video Amplifier circuits (via the front-panel LOG CAL control), is applied to pin 2 of switch U3063A through edge connector pin 51. Note that the internal video sections of switch U3063A are normally held energized (pins 2 and 3 connected, pins 15 and 14 disconnected) by the +5 V supply through resistor R3064. If the $\overline{\text{EXT VIDEO SELECT}}$ line (from the rear-panel ACCESSORIES INTERFACE connector, through edge connector pin 55) is grounded, the external video section of U3063A are de-energized. When this occurs, the EXT VIDEO signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57. This is shown in the simplified schematic diagram of Figure 7-14.

As shown in Figure 7-14, when no filtering is selected (all data bits are 0), either the internal or external signal is routed through U3062 and around the filter, because the two sections of U3063B is selected by DB1. When DB 1 is high, the video is routed through the some filter value will be selected by bits 2, 3, and 4. These data bits control three sections of switch U2015B to add or delete filter time constant.

The filter consists of resistors R2023, R2021, R2022, and capacitors C3026 and C2016, connected between U3062 and U2066. Table 7-6 lists the filter components in the circuit for each of the six bandwidths. Data bits 2, 3, and 4 are applied to switch U2015B (pins 8, 16, and 9) which selects the components. From U2066, the signal is routed through contacts 7 and 6 of switch U3063B to edge connector pin 57 as the VIDEO FILTER OUT signal.

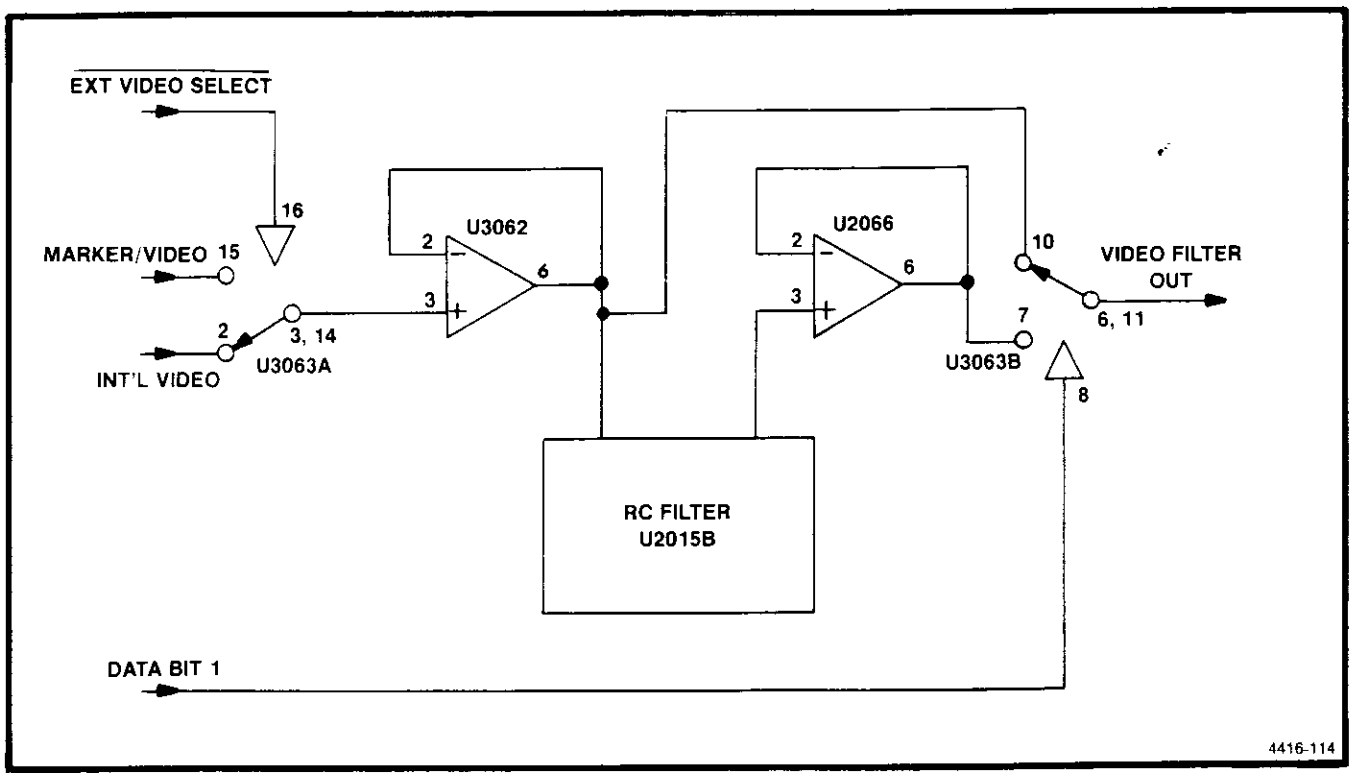


Figure 7-14. Simplified diagram of a video filter.

Table 7-6
FILTER COMPONENT COMBINATIONS

Bandwidth	DB=1	R2023	C3026	R2021	R2022	C2016
30 kHz	1	X	X	X	X	
3 kHz	1, 4	X	X	X		
300 Hz	1, 3, 4	X	X			
30 Hz	1, 2	X	X	X	X	X
3 Hz	1, 2, 4	X	X	X	X	X
0.3 Hz	1, 2, 3, 4	X	X	X		X

Video Blanking Circuits

The video blanking circuits allow selective blanking of the lower and upper ends of the local oscillator range. Selective blanking is required because the local oscillator sweeps the full span regardless of the band limits. The video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each and.

Video blanking and the PRESELECTOR DRIVE signal (which provides frequency information, in voltage form) are located on the Video Processor board. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. This feature allows the VIDEO FILTER OUT signal to be easily blanked at will.

This disable function is controlled by a combination of outputs from comparators U3015A and U3015B. Inputs to these comparators are from the PRESELECTOR DRIVE signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The PRESELECTOR DRIVE signal is applied from edge connector pin 54 through divider resistors R4013 and R4012 to the minus input side of U3015A, and through divider resistors R4014 and R4011 to the plus input side of U3015B. These dividers reduce the +10 V to −10 V excursion of the drive signal to +2.5 V to −2.5 V, which is the maximum input level to the comparators.

Input to the plus side of U3015A is from divider resistors R3011, R3012, and selected resistors R4024, and R4015. The inclusion of R4024 is controlled by DB5, through pins 15 and 14 of U3025, and R4015 is added by DB 7, through pins 2 and 3 of the same switch. The junction of divider resistors R3011 and R3012 may be connected to −5 V through R4024 or to ground through R4015. Refer to the Video Blanking table on the schematic diagram for data bit states for different bands.

Input to the minus side of U3015B is from divider resistors R4018, R4017, and selected resistor R3028. The inclusion of R3028 is controlled by DB6 through pins 10 and 11 of U3025. The junction of R4018 and R4017 is connected to +5 V through R3028 when it is selected.This switching arrangement of negative and positive levels for comparison with the reduced PRESELECTOR DRIVE signal enables the top and bottom extremes of the frequency excursion to be blanked. The blanking is activated by the disable function of switch U3063, which is microcomputer controlled.

DIGITAL STORAGE

The Digital Storage circuits select the display and process methods for information contained in the digital storage memories. This includes determination of the highest amplitude that occurred during a selected period (Max Hold mode), storage of a signal for later examination (Save A mode), subtraction of one signal from another (B−Save A mode), signal averaging (Averaging mode), and signal comparison (View A and View B modes). Two memories are used independently in these operations to store two complete signals that are each digitized at 512 points across the sweep. Therefore, two signals may be observed simultaneously or processed in separate ways.

In the Max Hold mode, the highest amplitude at each of the 1024 points in successive sweeps is stored and displayed. In the Save A mode, a signal is stored in one memory for later examination, and is not updated. In the B−Save A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored, but continually updated. In the averaging mode, the display area is divided by a horizontal cursor. Signals above the cursor are peak detected and displayed, and signals below the cursor are averaged. In the View A and View B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common. One such graph has a single Y value for each X value. An alternate presentation of the data in this graph would be a table simply listing the X coordinate values along with a corresponding Y value for each X value. To further simplify the graph, if the first X value and the spacing between X values were known (all spaces assumed equal), the two-column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This is the essence of digital storage—to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by the analog sweep voltage (X coordinate value) binary conversion. Once a set of binary numbers that represent values across a waveform is stored to create a table, the waveform can be recreated at any time by conversion of the table values (Y) and positions (X) back to analog voltages that represent amplitude and sweep positions.

The digital storage system uses a Table A and a Table B. Table B is updated every sweep. Table A is also changed unless the Save A mode is selected. There are 512 A values and 512 B values. The spacing between values is the same throughout both tables, but the starting point for Table B is shifted slightly so that when both tables are read, the readout values are interlaced.

When the signals are recreated, the contents of either Table A or Table B can be displayed, or both tables A and B can be displayed. If both Tables A and B are to be displayed, and the Save A mode is selected, the contents of both Table A and Table B are drawn, each display in its own trace. If the Save A mode is not selected, the contents of both Table A and Table B are displayed on one trace, with 1024 value positions across the screen. A third trace option is also available. In the B−Save A mode, the displayed values are those that result from an arithmetic operation and are the difference between the contents of Table A and Table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm determines the Y value to be stored for a particular X value. This allows the operator to select one of two methods to determine Y values; peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples, and there may be as many as 2^{17} samples. From this set of samples, either the largest sample value (peak value) or the mean of all the samples (average value) can be selected. Selection between peak and average is controlled by the front-panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/$\overline{\text{AVG}}$ logic signal. When the input signal is below the level selected by the front-panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This marker line is created when the dc level to the analog output line is switched during the marker cycle to produce the MARKER logic control signal.

Superimposed on the marker line is an intensified spot called the update marker, which indicates the X value at which new Y values are being computed for display update. The update marker is formed when the analog sweep input is compared to the display analog X output. When the two are the same value, the sweep is forced to pause, which increases the marker intensity at that point. Refer to the block diagrams adjacent to Diagrams 25 and 26.

U1023 and U2032 are the heart of the digital storage circuits. U1023 contains the vertical acquisition and display logic, peak detection, signal averaging, Z-Axis blanking, and special Y-value processing circuits. U2032 contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a programmable logic array system control matrix. The remainder of the digital storage control circuits consists of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and various auxiliary circuits. Timing is controlled by $\phi 2$ clock pulses (at 1 MHz) from the Processor board to the Horizontal Digital Storage board.

Vertical Section 

Vertical Control IC block diagram is shown in Figure 7-15. The vertical analog voltage is converted to a Y binary value by an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going $\overline{\text{SYNC}}$ signal. Most functions on both the vertical and horizontal control ICs are synchronized by this signal. On the negative-going transition of $\overline{\text{SYNC}}$, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the register on the negative-going clock transition. From the register, the output data is applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits; those that accumulate all of the Y values for a given X value into a grand total (called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, another 17-bit ripple counter is incremented to produce the denominator.

A division cycle is initiated when horizontal control IC U2035, detects a change in the X value. At that time it generates the ST DIV (start divide) signal. Upon receipt of this signal, and in synchronization with the $\overline{\text{SYNC}}$ signal, vertical control IC U1023 performs five functions (refer to Figure 7-15.

1. U1023 latches the current numerator in a 25-bit latch (25-to-1 data concentrator in Figure 7-15) and latches the denominator in a 17-bit latch (17-to-1 data concentrator).

2. U1023 clears the numerator adder circuits (25-bit summation register in Figure 7-15).

3. U1023 performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register.

4. U1023 loads the latched numerator and denominator serially into the divide circuit (subtractor in Figure 7-15) using the contents of the 25-bit shift register as a mask.

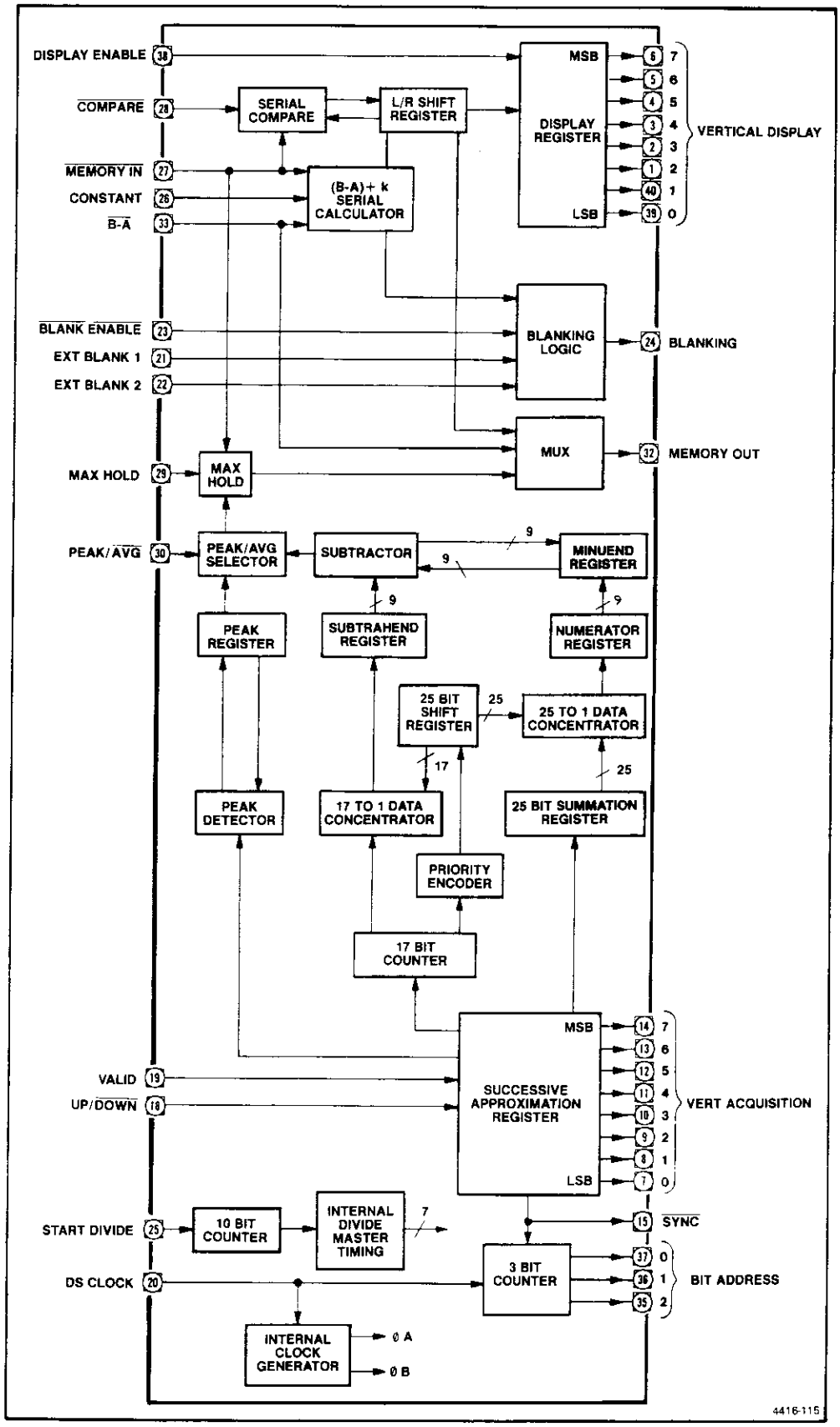


Figure 7-15. Vertical control IC, U1023, block diagram.

5. U1023 clears the denominator ripple counter (17-bit counter in the block diagram) to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse. The first bit of the quotient is available shortly after the first clock pulse that follows the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Since only 8-bit accuracy is required, with the priority encoder output used as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17- by 25-bit subtractor would be so long as to be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that questions whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PEAK/$\overline{\text{AVG}}$ signal. The selector output is routed through the Max Hold circuit, which functions in the same manner as the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values: the current memory value at the subject X coordinate or the previously-selected peak or average value.

Timing to set up the divide operation and clear the numerator, denominator, and peak circuit is controlled by a 10-stage Johnson counter. NOR gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses. Because the denominator is loaded into the divide circuit using a priority encoder, the most significant bit is always a 1. Space and power are saved by modifying the subtractor and not storing this 1.

All data enters and leaves the memory serially. Data read from memory enters an 8-bit shift register and, timed by the SYNC signal, is transferred to the vertical display output latch (display register on Figure 7-15).The same shift register is used for other purposes, so the DSPL EN (display enable) signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is seen in the B−Save A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed with the least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The shift register direction is reversed to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is (B−A)+K, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion when (B−A)+K results in an off-screen position, the subtractor blanks the display. (The subtractor examines the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.)

When the Save A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1024 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate (2^{17} samples). If this maximum value were in the B Table and the Save A mode was selected and B turned off, there would be an apparent drop in amplitude. For this reason, when the Save A mode is selected, a special set of circuits in U1023 compares all A and B values that have the same X value, and stores the larger in Table A. The B value is read and stored in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory. This operation is performed once each time that the Save A mode is selected.

Vertical control IC U1023 contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by U1023. All other addressing is performed by horizontal control IC U2035.

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U2033 to sample and hold switch U1033C. U1033C is controlled by flip-flop U1011B. Flip-flop U1011B generates the sample pulse, and is enabled during the clock cycle after the last sample, as indicated by the least significant bit from the successive approximation register in U1023. The switched sample is then applied through buffer U2032 to a summing junction. At this point, the output current from digital-to-analog converter U2024, that is supplied

from the successive approximation register, is subtracted from the sample current. The difference current is then applied through comparator U1031B and synchronizing flip-flop, U1017A, to pin 18 of U1023 as the UP/$\overline{\text{DOWN}}$ signal. The binary equivalent of the input sample is effectively produced by the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit.

Address Decoding. The address decode logic accepts inputs from the address bus and produces the control signals for read and write operations; $\overline{\text{CONT W}}$ (control write), $\overline{\text{DATA W}}$ (data write), and $\overline{\text{DATA R}}$(data read). The control write signal is used to gate the control word from the data bus into control register U1022 to generate mode control signals. This control word consists of five bits that represent front-panel functions. If output Q6 is low, a peak operation is forced; if output Q6 is high and Q7 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic, in general, performs control and interface functions between the active data circuits in the vertical and horizontal sections and the rest of the 494/494P. It allows the microcomputer to control the storage system functions and to access the digital storage memory. It also contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The microcomputer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U2021 is used to read data from memory to the data bus. Register U1021 is used to store information from the data bus for transfer to memory. Multiplexer U2016 performs the parallel-to-serial conversion and applies the data output to gate U2015B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U1023 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group on the Vertical Digital Storage board is the handshake logic that works with the horizontal control circuits to access the memory and to determine when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U2014B is triggered. This releases the BUS REQ (bus request) line to allow that signal to go high and signals the horizontal control circuit that memory access is required. When the horizontal circuits recognize the request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U1013A, U1013B, U2011A, and U2012A, and produces the low $\overline{\text{BUS GRANT}}$ signal to indicate memory access. The $\overline{\text{BUS GRANT}}$ signal then enables shift register U2021 to shift data from memory or enable register U1021. $\overline{\text{BUS GRANT}}$ also enables multiplexer U2016 to shift data to memory as indicated by the $\overline{\text{DATA R}}$ and $\overline{\text{DATA W}}$ lines. At the end of a data read cycle, gates U1012B and U2023C produce the $\overline{\text{INCR ADRS}}$ (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when the Max Hold mode is selected, the signal from Q5 of control register U1022 causes the circuits in U1023 to compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value. This causes the larger value of the two to be stored in memory. The signal from Q5, in combination with the VALID signal from the horizontal circuits, produces the MAX HOLD command to U1023 through buffer U2023E and gate U1025A.

Constant Circuit. As described previously, in the B− A operation, a constant is used. This constant is selected internally with switch S1014. This switch, in combination with multiplexer U1015, supplies the CONSTANT data to U1023. Multiplexer U1015 is, in turn, controlled by address bits 0, 1, and 2 to provide the proper constant data bit to U1023.

Output Circuits. From the U1023 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U1024. The converter output is then applied to the output storage/cursor switch, U1033B, through a vector generator that consists of an integrator (U1032 and C1031) with an associated feedback loop sample and hold circuit. Integrator U1032 has a time constant that provides a ramp to last between the existing sample and the new sample (that is, between sync pulses). Circuits U1033A and U1034 and capacitor C1038 make up a sample and hold circuit with U1034 acting as an output buffer. From U1034, the output current through resistor R1032 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch U1033B. U1033B, controlled by the MKR (marker) signal from the horizontal section, selects between the recreated video signal from U1032 and a dc (Peak/Average) level from buffer U2034, to be sent out as the vertical signal. The dc level is displayed only during retrace as the PEAK/AVERAGE cursor.

Peak/Average Level Circuits. The buffered PK/AVG LVL signal, from U2034, is compared with the sampled Video Filter Out signal, from U2032, by comparator U1031A. The output of U1031A is a high (1) if the Video Filter Out signal is greater than the PK/AVG LVL, or low if it is less. This output commands U1023, via U1025C and U1025D, to send peak or average data to the output. U1025B, C, and D are used if the instrument is under GPIB control to select one of three possible modes; Peak, Average, or front panel control knob.

Horizontal Section

Figure 7-16 is a block diagram for the Horizontal Control IC U2035. The horizontal analog voltage is converted to a current table value through a 10-bit tracking analog-to-digital converter, which consists of up/down interlock and 10-bit up/down counter in U2035, and external 10-bit digital-to-analog converter U2042. As the sweep moves right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, it generates a new X coordinate value (the D to A input) and a ST DIV (start divide) signal to start the storage cycle. The increment clock is the $\overline{\text{SYNC}}$ signal, and the decrement clock is the basic digital storage clock divided by two. When the Save A mode is selected, the counter skips every other binary number, so only B coordinates appear as addresses.

A programmable logic array ROM state device (PLA) provides the horizontal system intelligence. This PLA determines which trace is to be written on the screen, determines when to switch from read to write, generates the $\overline{\text{B-A}}$ coordination signals for vertical control IC U1023, controls the incrementing of the 9-bit display counter, and processes requests for the memory bus. The only one of these functions that is not obvious is the memory bus request.

When an external device elects to read from or write to memory, it allows the BUS REQ (bus request) signal to go high to request permission from the PLA. When the time becomes available, the PLA pulls the BUS REQ line low, which signals the start of a request cycle. For the next eight clock cycles, the internal multiplexer output lines are driven to the high impedance tri-state mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that either write to or read from memory. To generate X values to be written into memory, the circuits convert the sweep voltage to binary form. These circuits also count the sync cycles to cause the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter. This allows the counter to acquire the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to acquire the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the PLA. From the multiplexer, the output is applied to the memories as an address.

Address Registers and Buffers. Registers U2023, U2016, and U2014 perform address counting for bus transfer. These registers count INCR ADRS (increment address) pulses after having been reset to zero by the $\overline{\text{CONT W}}$ (control write) signal from the vertical section. From the address register, the outputs are applied to tri-state buffers U1023 and U1016 Then, the 10 bits of address from the counters are buffered as well as the DS R/$\overline{\text{W}}$ (digital storage read/write) signal line from the vertical section interface logic. Those signals are multiplexed onto the HD (horizontal display) lines and R/$\overline{\text{W}}$ (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data. At all other times, horizontal control IC U2035 outputs control the HD lines to determine the memory address for update of memory data.

Tracking Digital-to-Analog Converter. The 10-bit digital-to-analog converter operates as part of the loop that acquires a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U2042 accepts the output from the 10-bit up/down counter of U2035 and converts that output to an analog current. The analog current is then subtracted from the SWP signal (which is applied at edge connector pin 60 through buffer U2047B). The result of this subtraction is supplied to up comparator U1045A and down comparator U1045B. This creates the UP or DOWN signal, as appropriate to control the count direction of the 10-bit up/down counter in U2035. The counter then counts in the appropriate direction, which changes the digital-to-analog converter output to reflect the proper value. Overflow detector U1035 and underflow detector U1041 prevent the counter from counting too high or too low.

Update Marker Circuits. From U3025, the HD (horizontal display) signals are applied to 10-bit latches (U1022 and U1027) and clocked into the latch with DSPL EN. When DSPL EN is high, it indicates that the data currently in the vertical shift register in U1023, on the Vertical Digital Storage board, is to be displayed by shifting the data to the vertical display output latch in U1023. Lack of DSPL EN indicates that the display latches are not to be changed. The outputs of these latches are applied to 10-bit digital-to-analog converter U1042. The output current of the converter is applied through buffer U2047A, where it is converted to a voltage called HORIZ SIG. HORIZ SIG is a voltage that is sent to the Defelection Amplifier to deflect the crt beam horizontally when digital storage is being displayed. HORIZ SIG is compared to the sweep voltage in U2043. The output of the comparator is applied to a one shot multivibrator U1014A. The period of this one shot is determined by counter U2024, which is incremented by the rising edge of DSPL EN (display enable) from the PIA in the horizontal control IC U3025. The rising edge of the output from U1014A produces the INTENSITY signal that temporarily prevents counting by the 9-bit display counter in U2035. This effectively stops the beam for a short time and causes a bright spot on the marker trace (cursor) to indicate the X point being updated. Note that buffer U2047A also produces the HORIZ SIG (horizontal signal) that is sent to the Deflection Amplifiers.

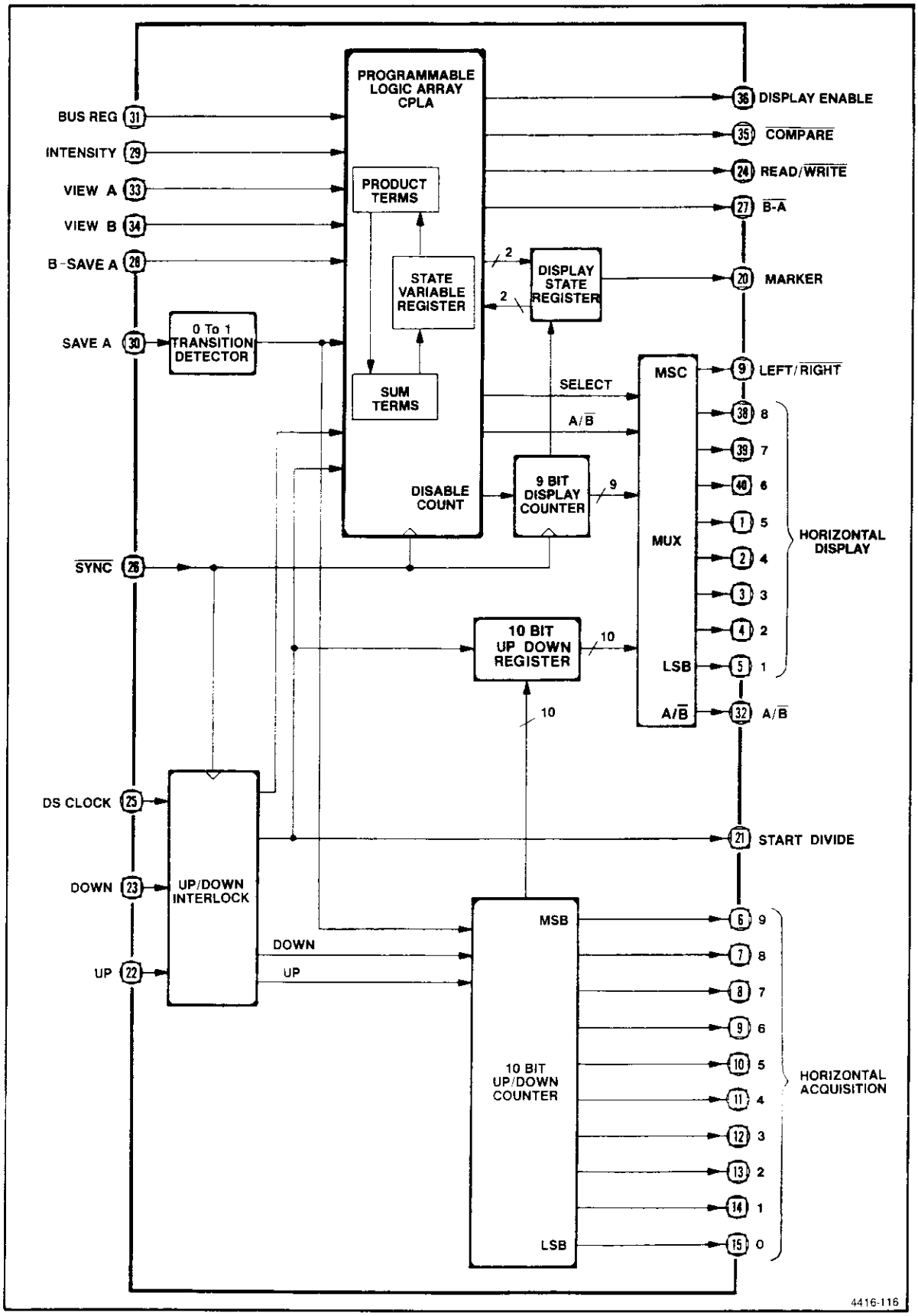


Figure 7-16. Horizontal control IC, U2035, block diagram.

Fast Retrace Blanking. Between the display of the B memory contents and display of the A memory contents, a fast retrace occurs. This retrace, unlike the one that follows the A memory display (cursor), is not required to be seen and is blanked. This is accomplished by blanking control flip-flop U1014B, which is controlled by the most significant bit of the memory address and the DSPL EN signal during a marker cycle.

Memories. Integrated circuits U1026 and U2026 provide 8 k bits of random access memory for storage of the 1024 data points used in the digital storage system. Addressing during bus transfer of memory data is controlled by address tri-state buffers U1023 and U1016 and by horizontal control IC U2035 during memory update.

DEFLECTION AMPLIFIERS ◈27

Refer to the block diagram adjacent to Diagram 27 as well as the schematic diagram. The Deflection Amplifier receives vertical signal information from the vertical section of Digital Storage or the Video Processor, and horizontal or sweep voltage from the horizontal section of Digital Storage or the Sweep board. Readout data for the display comes from the Crt Readout circuits. The output of the Deflection Amplifier drives the crt deflection plates. The amplifiers contain the switching circuits necessary to perform the selection functions and they also contain the amplifier stages needed to produce the deflection plate drive signals.

Horizontal Section

Signal lines HORIZONTAL SIGNAL, (from the digital storage circuits through edge connector pin 49) and SWEEP (from the Sweep circuit through edge connector pin 51) are applied to switch IC U7055A. U7055, under control of the STORAGE OFF signal (from the digital storage circuits through edge connector pin 7) selects either the HORIZONTAL SIGNAL or SWEEP input. The SWEEP signal is selected when the STORAGE OFF line is floating or pulled high. The HORIZONTAL SIGNAL is selected when the line is pulled low. Resistive divider R7051 and R7081 reduces the selected signal from 1 V/div to 0.5 V/div. U7073 buffers the selected signal. It goes out to the HORIZ OUT rear-panel connector via edge connector pin 48. U7073 applies the signal to switch U7055B. The HORIZ R/O signal, from the Crt Readout circuits, is also applied to U7055B. The R/O OFF signal, from the Crt Readout circuits selects between these two signals. When R/O OFF is floating or pulled high, the switch transmits the signal from buffer U7073 to the shaper. When the line is pulled low, it selects the HORIZONTAL R/O signal.

U7055B applies the signal to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R5059, R5058, R5057, R5062, R4061, and R4059, plus diodes CR4052, CR4051, CR4058, and CR4056. The HORIZONTAL POSITION voltage, from the front panel via edge connector pin 47, through resistor R6032, is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the deflection amplifier circuits. Horiz Gain adjustment R1055, calibrates the amount of gain compensation required for proper deflection sensitivity.

The horizontal deflection amplifier consists of two circuits similar to each other, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to Q4038A of the inverting side are through the parallel combination of resistors R4049 and R4048 and capacitor C4057. The series connection of resistor R4048 and variable capacitor C4057 provides high-frequency response compensation. Capacitor C2047 controls high-frequency feedback.

Input to the non-inverting side is through resistor R5029 to the base of Q4025A. R4019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. High-frequency feedback is controlled by capacitor C3021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates a gain-degenerated dual PNP transistor at the input side (for temperature compensation) connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037 and P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples the signal to the base of Q1049. Q1049 provides the positive drive to the deflection plate, and Q1043 provides the negative drive. Each output transistor can provide a 200 V excursion in approximately 1 μs.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031, R1052, and R1049 at the base and emitter of Q1049. Current through resistor R3031 also provides the current for the input stage, Q4038A/Q4038B. Emitter follower Q4047, operates at approximately 2.5 mA.

Resistors R1045 and R1034, in the emitter circuit of Q1049 and Q1043, degenerate the output stage for fast steps. Current from the −15 V source through resistor R4033, sets the output operating level. Feedback resistor R3045 sets this output level at approximately 142 V.

Operation of the right-hand (inverting) section is basically the same as the left-hand (non-inverting) section.

Vertical Section

VIDEO FILTER OUT, from the Video Processor, and VERTICAL SIGNAL, from the Digital Storage, are routed through switch IC U6055A, under control of the STORAGE OFF signal from the Digital Storage board. Note that the VIDEO FILTER OUT signal is buffered by IC U7065 to prevent a change in load transients from affecting the signal level. A high on the STORAGE OFF line selects the buffered VIDEO FILTER OUT signal, and a low selects the VERTICAL SIGNAL. U6065 inverts the selected signal and clamps it to ground. Both the VIDEO FILTER OUT and the VERTICAL SIGNAL are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline.

The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. Buffer U6073 supplies a sample of this centered signal to the rear-panel VERT OUT connector via edge connector pin 46. The output of U6073 is also applied through switch U6055B, when the R/O OFF line is high, to the vertical shaper circuit. When R/O OFF line is low, the VERTICAL R/O signal is applied to the shaper.

The vertical section shaper (R4062, R4065, R4067, R4069, R4064, and CR4063, CR4064, plus the preamplifier U2062) operates the same as the horizontal section. Q4078 limits positive excursions to approximately one division above the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages, with the exception of higher bias current. Current flow of approximately 1 mA, through resistors R3089 and R3098, produces approximately 5 mA in the output stages. To correct for the increased current in the dual input stage transistors, Q4083 and Q4101, resistors R5081 and R5099 are lower value than their counterparts R5041 and R5027 in the horizontal amplifier.

U6024 compares the signal level from the baseline clamp, U6065, with a reference level set by divider R7032/R7034. This produces the CLIP signal for the Z-Axis interface circuits. When the VIDEO FILTER OUT signal is more negative than the reference level (approximately 1 division above baseline), it pulls the CLIP line low. R7021 pulls the CLIP line high if the signal is more positive than the reference level.

Z-AXIS AND RF INTERFACE BOARD ◈28

Refer to the block diagram adjacent to Diagram 28 as well as the schematic. The Z-Axis and RF Interface board contains the RF interface circuits, crt Z-axis drive circuits, power monitor circuits, and a timer that measures operational hours. This board provides beam intensity (nominally from the front panel), baseline clipping, and unblanking logic for the signals or readout data. Unblanking logic comes from the Sweep board, the Crt Readout, the Deflection Amplifiers, and the Digital Storage. The RF Interface circuits receive data from the microcomputer that controls the RF Attenuation, transfer switch, and IF selection. A power fail circuit on the board detects any change in input power frequency or power supply voltage and notifies the microcomputer. An elapsed time meter is also located on the board to give a indication of total instrument operating time.

RF Interface Circuits

The RF interface includes the digital control circuits that receive the address and instruction data from the microcomputer and decode it to control the RF Attenuator, Transfer Switch, and IF selection. The power supplies that are required to drive the attenuator and switches are also included.

Digital Control. Address decoder U2045 latches the data at the input of U3046 whenever the microcomputer selects address 4F. Table 7-7 lists the purpose of each data line from the buffer.

Table 7-7
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enables current drivers Q2025 and Q3028
Q5	Enables transfer switch driver
Q6	Selects 829 MHz IF (high state) or 2072 MHz IF (low state)
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

When Q4 of U3046 goes low, Q2025 and Q3028 conduct. This raises the Vcc of attenuator drivers U3034, U3029, and U3038 to +16 V for approximately 100 ms to energize the attenuator solenoids. A diode protects each attenuator driver output line from the inductive voltage surge that occurs when the solenoids change state.

Transfer Switch. Operation of the Transfer Switch is dependent on the output of Q3025/Q3024. The Q5 output of U3046 is applied to the input of operational amplifier U4023, which drives differential amplifier Q2025/Q3024. When Q5 goes high, Q3025 is biased on and the Transfer Switch selects the external mixer. When Q5 goes low, Q3024 is biased on, and the internal mixer is selected. Diodes CR3018 and CR3017 protect the transistors from voltage spikes induced when the Transfer Switch changes state.

Z-Axis Circuits

The Z-Axis circuits provide the drive currents and bias voltage to operate the crt. They consist of the intensity control logic circuits, which control the crt beam current for normal signal display operations, and the unblanking gates, which furnish current to the Z-Axis drive amplifier to drive the crt control grid.

Z-Axis Drive Amplifier. The Z-Axis Drive Amplifier is an operational amplifier that consists of transistors Q3047, Q4058, and Q4059, and related components. R1050 is the input resistance for the amplifier, and R2066 is the feedback resistor. The output is clamped by diodes CR3059 and CR3066 to protect the amplifier from transient surges in case of crt arcing. The amplifier is driven by two sources, exclusive of each other; U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. U2039 is an AND-NOR gate that provides the logic to one input of NAND gate U2038A to turn Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 7-8 lists the conditions under which U2039 will output a high to U2038A.

Table 7-8
U2039 TRUTH TABLE

	Condition
U3046 output (line Q8)	0 0 0 1 1 1 0 0 0
CLIP	0 0 0 0 0 0 1 1 1
Z-Axis Blank	1 1 1 1 1 1 1 1 1
Storage Off	0 0 1 0 0 1 0 0 1
SWP GATE	1 0 1 1 0 1 1 0 1
U2034, pin 10	0 0 0 0 0 0 0 0 0

Only the combinations shown in Table 7-8 plus a high on the R/O OFF line will gate a low out of U2038A. When the U2038A output is low, emitter current is furnished to Q2044, which in turn furnishes current through R2051 (the input resistance of the Z-Axis drive amplifier) to Q3047. U2034B is a single-shot multivibrator that produces a 3 μs pulse to blank the crt beam during trace return, between readout and signal display.

The other source of input current to the Z-Axis drive amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and R/O OFF is low.

Q1028 is the current source for divider R1030/R1025 that establishes the operating point for Q2042 and Q2044, which sets the intensity level. Diodes CR1045 and CR1043, connected from the base of Q2042 and Q2044 to the emitter of Q2022, limit the display intensity. These diodes prevent the bases from going more positive than approximately 0.6 V above the emitter voltage of Q2022. This circuit, which includes Int Limit adjustment R1027, sets the maximum current for both Q2042 and Q2055.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. Trace Rotation adjustment R1021 sets the current so the displayed trace is aligned with the graticule.

Power-Fail Detector

This circuit detects an instrument power failure and transmits the information to the Processor and Memory boards. The LINE TRIGGER signal from the Power Supply board through edge connector pin 60 is supplied to Q2011. Q2011 buffers the signal and applies it to the input of retriggerable one-shot U2034A. U2034A performs as a missing-pulse detector to generate a power-fail signal through Q3011 to notify the Processor and Memory boards if more than two 60 Hz cycles are dropped. To avoid an undefined state, the output from U2034A is latched low by U2051. Under normal operating conditions, the $\overline{\text{POWER-FAIL}}$ signal from Q3011 is high.

Power-Supply Monitor

This circuit detects if one or more of the instrument power supplies have failed. Each voltage supply in the instrument is fed into thick film resistor network R3051, which balances the currents to provide a null output (approximately 1 Vdc). Any line change of more than ±25% drives the input to window comparator U3051 beyond its ±200 mV threshold and generates a low output. Q2059 and Q2067 drive the dual light emitting diode DS1062 to provide visual indication of power-supply status (green indi-

cates normal operation and red indicates a fault condition). The output of U3051 is also fed to tri-state buffer U3052. After instrument power up or if a failure is detected, the microprocessor will poll address CF to determine power-supply status over the data bus.

Timer

An electromechanical timer, M1019, is calibrated for a duration of 5000 operating hours. The current through R1015 and the timer causes the copper band to progress along the scale.

HIGH-VOLTAGE SUPPLY 29

Refer to the block diagram adjacent to Diagram 29 as well as the schematic diagram. The High-Voltage Supply furnishes the −3860 V crt bias and 6.3 Vac filament voltage to the crt cathode, and provides dc restoration for the Z-AXIS DRIVE signal. The supply consists of the following four main circuits:

1. The high-voltage oscillator circuit produces the crt filament voltage and the 200 Vac that is stepped up and applied to the voltage doubler circuit.

2. The voltage doubler circuit rectifies and filters the high voltage for application to the crt cathode.

3. The high-voltage regulator circuit samples the high voltage and regulates the operation of the high-voltage oscillator.

4. The Z-Axis clipper and rectifier circuits couple the Z-AXIS DRIVE signal to the crt control grid.

High-Voltage Oscillator. This circuit consists of transistor Q1073, transformer T2065, and associated components. The approximately 200 Vac, oscillator output is coupled across T2065, where it is stepped up for application to the voltage doubler, and stepped down for application to the crt filament.

Voltage Doubler. The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode through the filter consisting of R3038, R1039, and C4024. Reference voltage for the regulator is also taken off the end of R1039. R1039 keeps the filament at the same potential as the cathode.

High-Voltage Regulator. This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider that consists of R1017B and R1017C. This voltage divider is connected through R1042 to +15 V. The sample of the high voltage at pin U is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied as bias to Q1073 to set the oscillator current.

CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The high-voltage oscillator is protected by CR4071, R3079, and R4074 in case the +100 V supply should fail. Normally, CR4071 is back biased. If the +100 V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin to oscillate only after the 100 V supply reaches a voltage sufficient to sustain oscillation. CR3077 (in the regulator output circuit) protects the base of Q1073 from excessive negative voltage.

Z-Axis Clipper. This circuit consists of diodes CR1056 and CR1046, plus associated components. The 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit, that consists of VR1041, R2050, R2040, and Q2048 holds holds the cathode of CR1046 at approximately +100 V to 143 V, depending on the setting of R2040. CR1046 and CR1056 clip the incoming 225 Vac to a total excursion of ($V_{CR1046\ cathode} - V_{Z\ AXIS\ DRIVE} + 1.2$ V). R2040 is adjusted for complete cut-off of crt with Z-Axis DRIVE at minimum. The voltage that passes the clipper circuit is coupled through C1031 to the Z-Axis rectifier.

The clipped Z-AXIS DRIVE signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. The crt grid is protected from high-voltage arcs by neons DS2052, DS2054, and DS2057. R1043 protects CR2046 and CR2044, respectively, from high-voltage surges if the crt should arc.

CRT READOUT 30

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display those characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41 MHz, supplied by the Processor board. The readout circuitry (Figure 7-17) is composed of the following elements.

1. Readout On Timing—RAM for character storage.

2. Character Counter—to access the RAM and control the scan.

3. Character Generator—to unblank the crt beam.

4. D/A Converters—to deflect the crt beam.

5. Instrument Bus Interface—to store characters and control the display. A more detailed block drawing is provided adjacent to Diagram 30.

Forty (40) characters can be displayed per line, with up to 16 lines selected, under software control. Normally, up to three lines are displayed while simultaneously displaying the spectrum. When over three lines are to be displayed, the spectrum display is disabled in order to keep the readout refresh rate above 60 Hz.

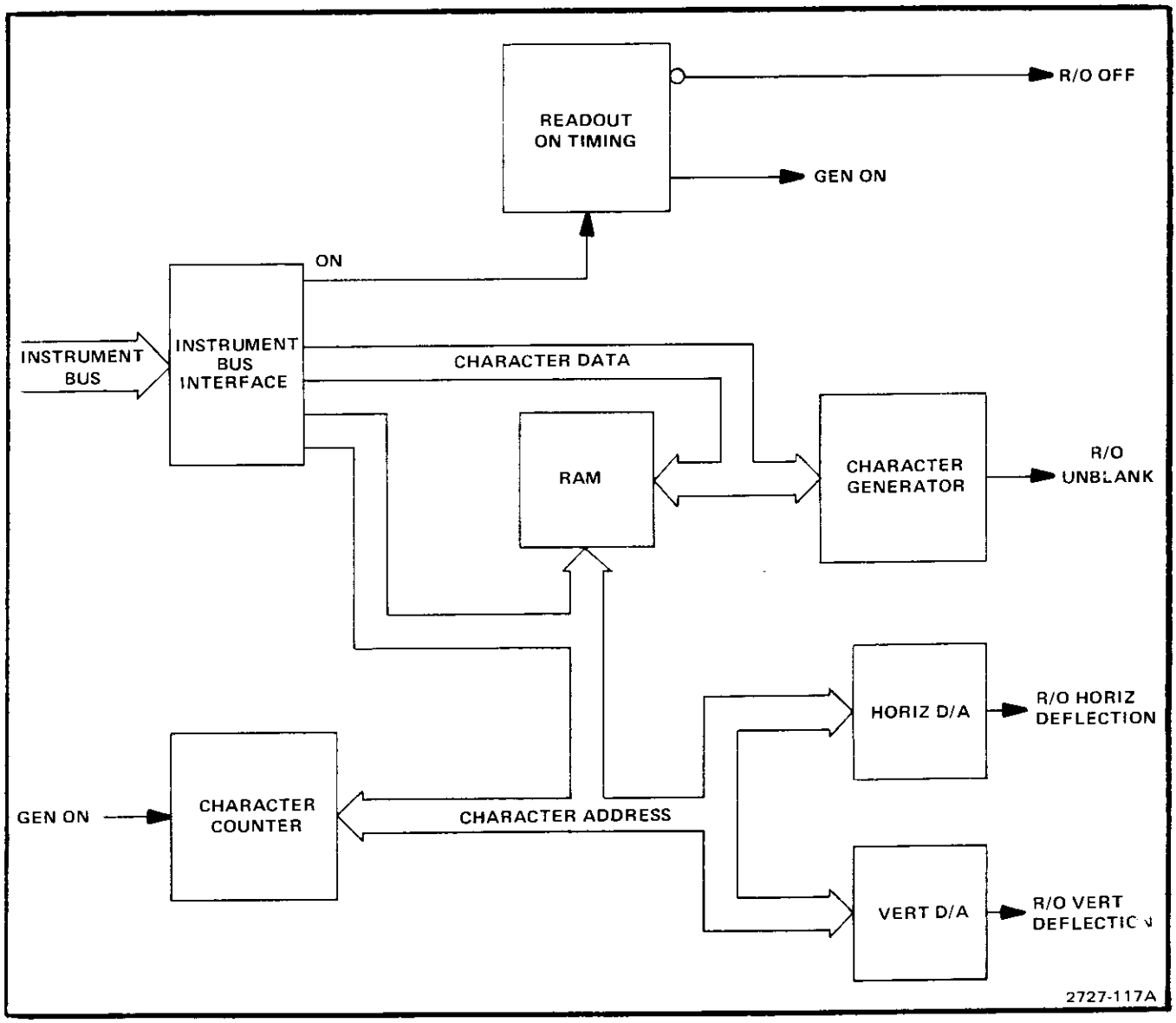


Figure 7-17. Block diagram of crt readout.

Readout-On/Off Timing. Characters are written one at a time. This allows a portion of the spectrum to be drawn between each character. The character duty cycle is between 10% and 25% because it varies with the character drawn. The time sharing between character writing and spectrum display is pseudo-random to reduce the effect of gaps in the spectrum display by moving them on the trace.

The readout-off time is set to 140 μs by one-shot multivibrator U1055 (Figure 7-18). Flip-flop U1041B asserts GEN RUNNING after U1055 times out, allowing a character to be drawn. After a character is written, $\overline{\text{ROW 0 COL 0}}$ resets the flip-flop, which clocks off time one-shot U1055. The ON control bit must have been asserted by the microcomputer to get readout (as described under Instrument Bus Interface later in this section).

If BLANK (MSB of the character data) is not set, the GEN RUNNING flip-flop unasserts R/O OFF through OR gate U2044B; this switches the readout deflection signals for the deflection amplifier inputs (Diagram 27). BLANK can be set by the microcomputer to load a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC, U2048, is often used in raster scans, in this application it is used to write complete characters, as shown in Figure 7-19. A character is drawn as a pattern of dots in an 8 x 8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

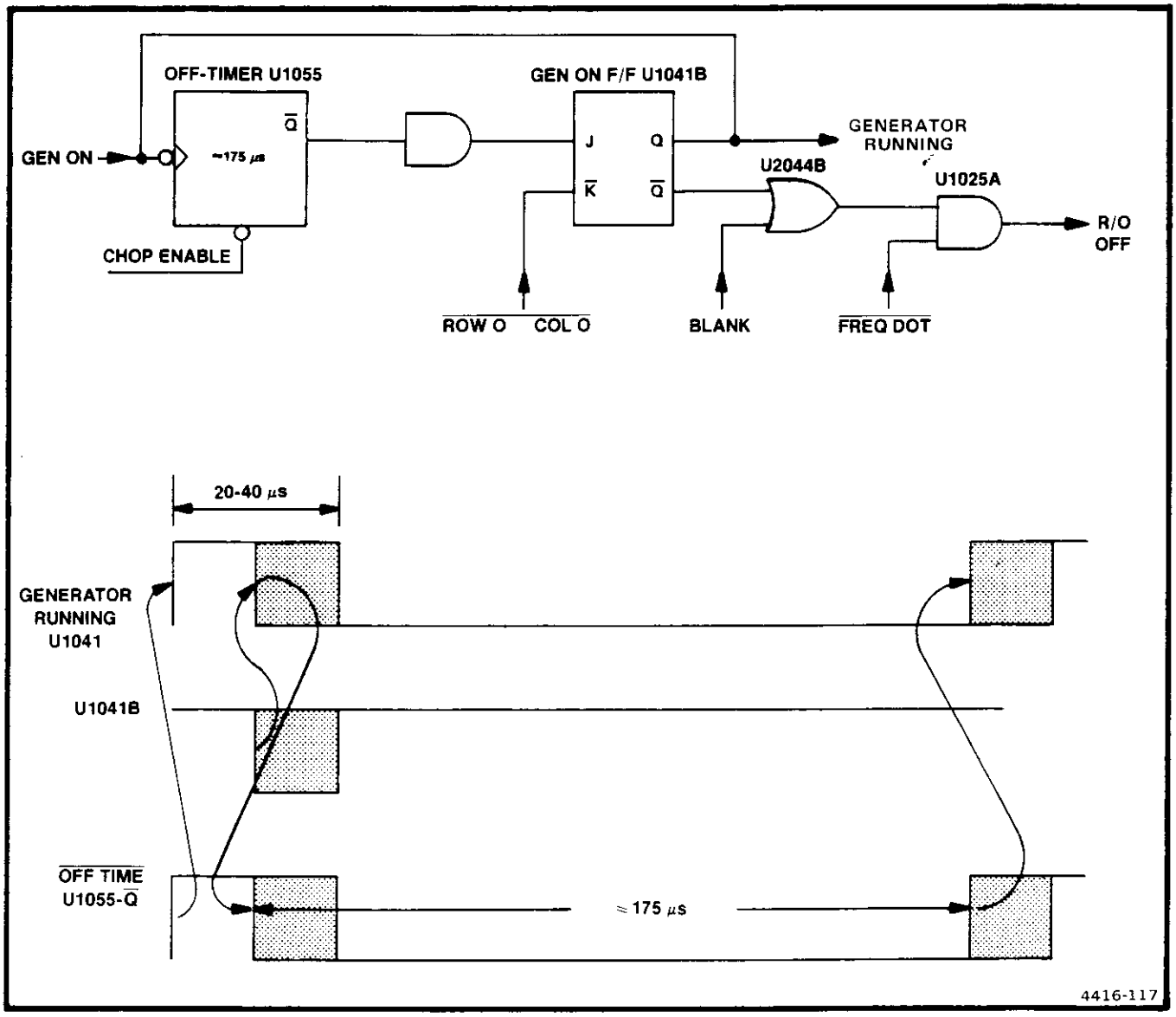


Figure 7-18. Character on/off timing.

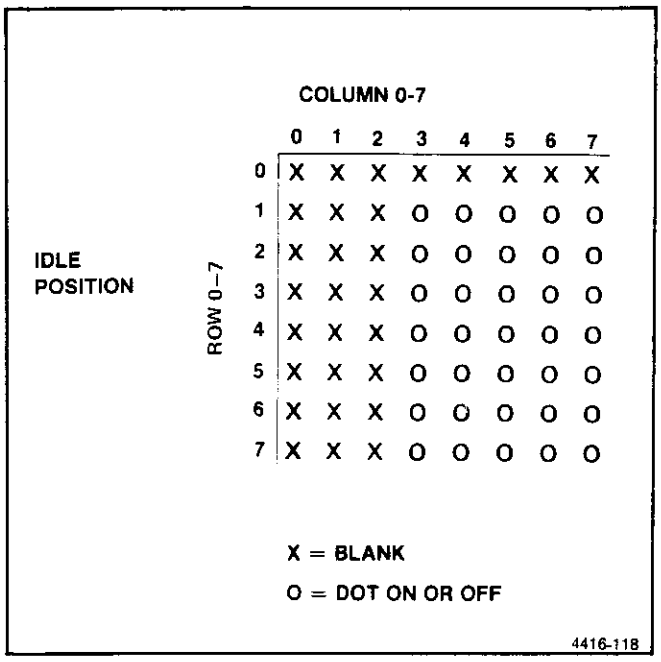


Figure 7-19. Character scan.

Character counters synchronize the horizontal and vertical scan with the Z-Axis signal from the character generator IC to draw the character. These counters, U2022, U2018, U2026, and U2014, are wired to divide by 8 for the columns within a character (columns A, B, C), divide by 8 for the rows within a character (rows A, B, C), divide by 40 for the characters within a line (characters A, B, C, D, E, F), and divide by 16 for the lines within a display. The counters are enabled only when the generator has control of the crt beam (GEN RUNNING line asserted) and INCR (increment) is high (when INCR is low, the crt beam is stopped to write a dot on the crt).

The SKIP line from U2052 permits software control of the allowable states of line counter U2014. By placing a one in this bit of a character, the line counter is allowed to count up to the next state. This will continue until a character is encountered with the "skip" bit set to zero. This allows the addition of a third line to the normal two-line readout for status messages, by operating with the circuit normally in the 16-line mode (all but the bottom and top lines start with a readout character of 40 hex, which has the SKIP line set high). Thus, all but the bottom and top lines are skipped. When large messages are to be displayed, the SKIP line is set low for all characters and 16 lines are displayed.

The counters are wired to force the D/A converters to step through the character horizontally, a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U2039B and U2031. The AND gate and decoder combine to control the character generator, U2048, which generates the correct pattern of blanking to draw the pattern of dots for the character. U2048, the 8678 character generator IC (Figure 7-20) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repertoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed, one 8-bit line at a time, into a shift register that is clocked out one bit at a time to control the crt Z-axis.

Character Generator Timing. The character generator timing lines are called DOT, LINE CLK, $\overline{LE}$, and $\overline{CLR}$. Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE CLK switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on $\overline{LE}$ (load enable), setting up the shift register to display another row of dots. $\overline{CLR}$ resets the line counter to begin drawing another character.

GEN RUNNING, INCR, and CRT CLK are combined through AND gate U1037B to generate DOT to clock the character generator, U2048. Inversion by the gate restores the phase relationship of the DOT input and the inverted LINE CLK. $\overline{LE}$ is gated by U2039B when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE CLK advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. Decoder U2031 outputs a $\overline{ROW\ 1\ COL\ 1}$ when the character counter reaches row 1, column 1 (the first non-blank row of dots scanned in each character). This is asserted once during the scan of each character.

The sequence of events to scan a character is illustrated in the character timing diagram (Figure 7-21). At 1, the character generator finishes a character. Then, when the counter advances, decoder U2031 asserts $\overline{ROW\ 0\ COL\ 0}$, resetting the GEN RUNNING flip-flop, U1041B, on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When readout-off time one-shot U1055 completes the time-out period, it allows the GEN RUNNING flip-flop to be set. Just before the scan enters the actual character clock area (at 6), $\overline{CLR}$ resets the character generator line counter (at 5). $\overline{LE}$ (at 5a) loads one row of dots into the output shift register so that the first dot is output at 6. The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 5 x 7 character matrix; 0 for a blank and 1 for a dot that is to be written. As the scan progresses at 3.4133 MHz, a rather faint character display might be expected. To brighten the dots that are written, a shift register is used as a delay element so that dots are displayed and counters disabled for 3 clock cycles.

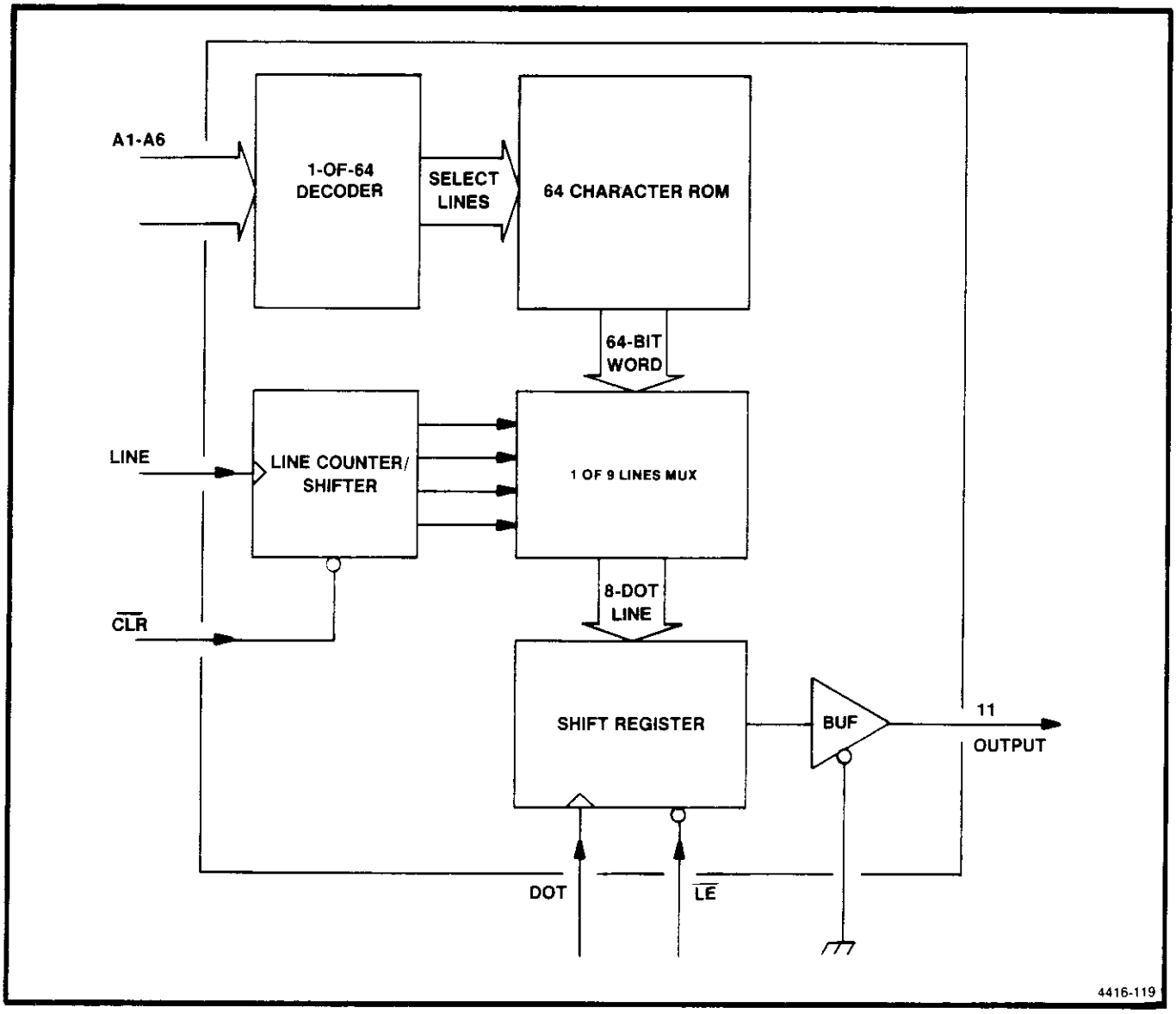


Figure 7-20. Character generator (U2048) block diagram.

Assume that no dots have been displayed for several dot clock cycles, so the output of the character generator, pin 11 of U2048, is low. Thus, U1020B output is high, and the outputs of the delay shift register U1025C and U1020B are low. When a dot is displayed, the character generator output (pin 11 of U2048) goes high. This causes INCR to go low and disable the counters. It also causes the input to the delay shift register, pin 11 of U1020B, to go high. On the next clock pulse, U1020A output follows INCR and goes low. The shift register clocks the one in, and the unblank flip-flop, U1016B, goes high, turning the crt beam on. This is the only "1" it will clock in, because the output of U1020A is now low. The circuit is now in a lock-up state with the counters disabled. Two more clock cycles will go by until the "1" in the shift register is clocked out, allowing the output of U1033C to go high. A high on the output of U1033C starts the counters again and resets unblank flip-flop U1041A.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports.

Port	Hex Address
Control/Address	5F
Address/Data	2F

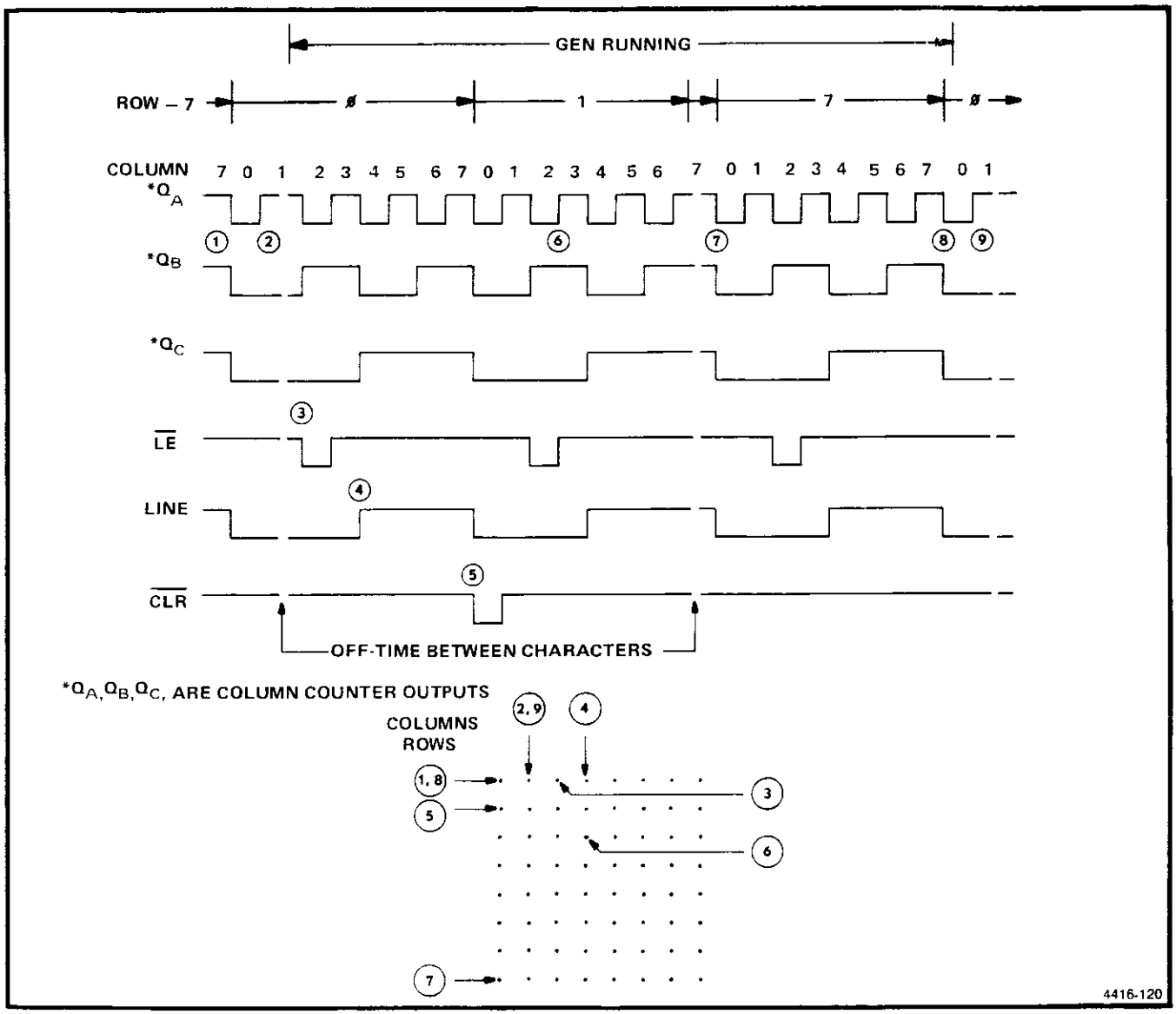


Figure 7-21. Character timing diagram.

Decoder U3051 asserts 5F when it sees a value of 5 on the upper four bits of the instrument bus address lines, and 2F when it sees a value of 2. The decoder must be enabled by DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

Control Port. The control address port, U3034, turns the readout on or off, steers data sent to the address/data port, controls the mode of the frequency marker dot, and contains two bits of the RAM address. The bits are defined in Table 7-9. Bit numbering on the instrument bus starts at zero. However, the D and Q pins of U3034 (and some other ICs) are numbered in accordance with their data sheets, starting at one.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit releases $\overline{\text{CLEAR}}$ from the GEN RUNNING flip-flop and allows the off timer, U1055, to set U1041B. Also, when the ON/OFF line goes high, it enables the INCR gate, U1037C, to steer the position counter onto the character RAM address inputs through line driver U3042 and multiplexers U1050 and U1046. When cleared, this bit places an address, latched in U3038 and U3034, on the

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, Q8 of U3034 gates a high on the output of U2044A. This high prevents input to the character RAMs, U2057 and U2052, by setting its R/$\overline{W}$ input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U3047; meanwhile, U2037A is enabled to gate the clock signal that latches the address. The positive clock transition is applied to U3038 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing $\overline{2F}$.

When this bit is cleared and $\overline{2F}$ is asserted, U2044A enables the character RAM for input and passes the data through U3047.

Table 7-9
CONTROL PORT

Bit	Function
0	Readout on/$\overline{off}$
1	Address/$\overline{data}$
2	A9 of RAM address
3	Max Span dot
4	A8 of RAM address
5	$\overline{16}$ line mode
6	$\overline{40}$ characters/line
7	Spectrum display available

Bit 2 is the MSB of the RAM address.

Bit 3 controls the frequency dot marker. This bit is set in the MAX SPAN mode to position the frequency dot with BFRD TUNE VOLTS from the first local oscillator. When cleared, this bit centers the frequency dot on the spectrum display.

Bit 4 is the A8 address line for the character RAMs.

Bit 5 is the select for 16 lines mode.

Bit 6 selects the 40 character/line mode.

Bit 7 enables the clipped display with the spectrum. When high, U1055 is enabled and causes 140 μs periods to occur between characters when the spectrum is disabled. When low, U1055 is disabled, R/O OFF is forced low to disable the spectrum display, and W1028E forces the current boost addition to be disabled. Also, U1016 is disabled so that the marker dot is not displayed.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires the following four write cycles.

1. Bit 2 in the control port is set for an address transfer, and the upper 2 bits of the RAM address (A8, A9) are sent.

2. The lower 8 bits of the address in the character RAM are sent to the address/data port.

3. Bit 2 in the control port is cleared.

4. The data is sent to the address/data port. The bits are defined in Table 7-10. Bits 0-5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 7-10
ADDRESS/DATA PORT

Bit	Function
0-5	Address pf ASCII code
6	Skip bit
7	Blank character

Bit 6 causes the line counter, U2014, to skip a line, if set.

Bit 7 is used to reduce overhead readout display. It is set when a space is transferred to the character RAM, so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN RUNNING flip-flop from gating R/O OFF low through U2044B.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

The negative transition of line D triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Figure 7-22.

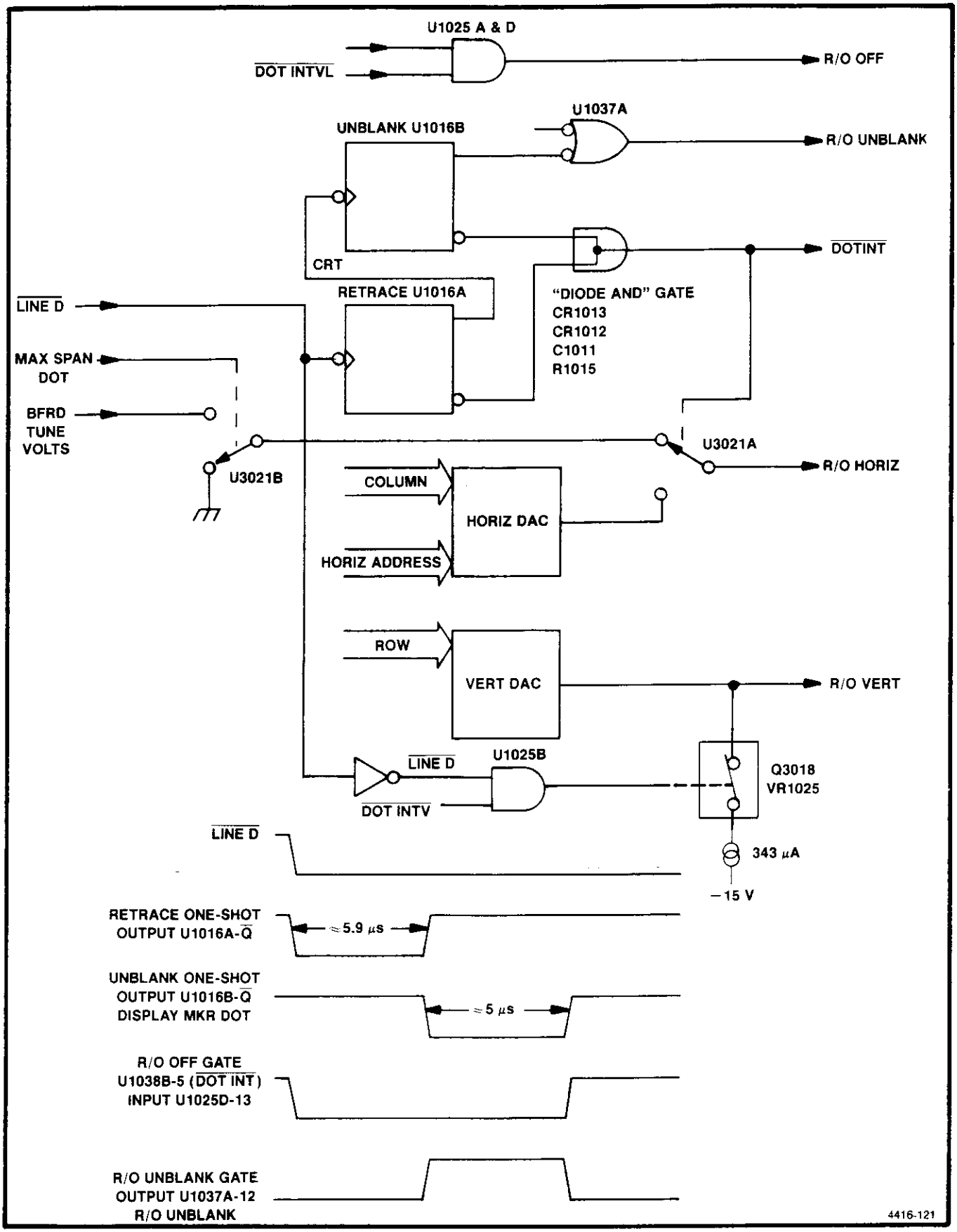


Figure 7-22. Frequency dot marker simplified diagram with timing waveforms.

U1016A delays the marker dot to allow retrace while gating $\overline{\text{DOT INV}}$ low to set up the display. $\overline{\text{DOT INV}}$ affects the readout deflection outputs in the following ways.

1. The horizontal output is connected either to ground, for a center-screen dot, or BFRD TUNE VOLTS, for a max span pointer. BFD TUNE VOLTS is proportional to the center-frequency readout offset from the center of the frequency range.

2. The U1025B output goes low during the dot interval to cause Q3018 to insert an offset current into the vertical output, to shift the dot position down on the screen.

3. R/O OFF is gated low to switch the deflection amplifier inputs from the Trace Mode to the Readout Mode, using the marker dot horizontal and vertical signals.

When the retrace one-shot times out (approximately 5.9 μs), it's Q line triggers the unblanking one-shot U1016B, which sets R/O UNBLANK high for approximately 5 μs, via $\overline{\text{DISPLAY MKR DOT}}$ through U1037A. This refreshes the dot. $\overline{\text{DISPLAY MKR DOT}}$ also holds $\overline{\text{DOT INTVL}}$ low through CR1013, until the dot marker is drawn. R1015 and C1011 slow the rise of $\overline{\text{DOT INTVL}}$ to prevent a spurious signal through the "diode AND" gate.

FREQUENCY CONTROL SECTION 

The Frequency Control section performs the tuning and scan function for the Preselector, 1st LO, and 2nd LO. It also provides the sweep voltage for the deflection amplifiers in the Display section so the crt display is coincident with the frequency scan and tuning. This section contains the following major circuits.

Sweep. Circuits on the Sweep board accept trigger inputs from line, internal and extenal sources, and the normal free-run mode of operation. They also receive external horizontal and manual sweep inputs. The circuits produce a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt beam across the horizontal axis and drive the horizontal portion of the digital storage circuit, plus a ramp (OSC SWEEP) that is fed through the Span Attenuator to the Preselector Driver, the 1st LO Driver, and the 2nd LO.

Span Attenuator. This circuit attenuates the ramp signal as required, to sweep the frequency of the 1st and 2nd local oscillators, and tune the Preselector so it tracks the center frequency.

Center Frequency Control. The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the microcomputer, so remote control of the frequency is possible, by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the Preselector Driver for summing with the IF Offset voltages, and to the 2182 MHz Phase Locked 2nd LO circuit for summing with the 2nd LO SWEEP signal.

1st LO Driver. The 1st LO Driver performs the following: 1) combines the COARSE TUNE VOLTS signal with the SPAN signal and outputs a current to drive the 1st LO; 2) produces the tuning and sweeping signal for application to the Preselector Driver circuits; 3) produces the mixer bias voltages; 4) produces the BUFFERED TUNE VOLTS signal that is applied to the Display section; 5) produces a reference voltage that is used in both the 1st LO Driver circuit and the Preselector driver; 6) produces a supply voltage for the 1st LO.

Preselector Driver. The Preselector Driver combines the FINE TUNE VOLTS signal,from the Center Frequency Control board with the PRESELECTOR DRIVE signal and the SPAN VOLTS signal from the 1st LO Driver. This combined signal is offset, to compensate for the selected 1st IF, then shaped so the Preselector tracks with the 1st or 2nd LO as it is tuned by the output current. The Preselector Driver also drives the Filter Select switch that selects either the Preselector or the Low-pass Filter, depending on the frequency band selected.

SWEEP

An overall block diagram of these circuits appears adjacent to Diagram 31. The circuits on this board provide the ramp voltage that drives the horizontal deflection amplifier, the 1st LO Driver and the Preselector Driver, and the 2nd

LO. The sweep board also provides signals for the Z-Axis circuitry, an external plotter pen, digital storage, and it is the interface between the microcomputer and the Reference Lock module located on the RF deck.

Three instrument bus addresses are associated with the sweep board. Address 0F and 1F are write addresses and 9F is a read address.

U3032 is the instrument bus address decoder and outputs a low on the appropriate pin if address 0F, 1F, or 9F is selected. U2032 is an eight bit register (D flip flops) which retains data written on the data bus at address 0F. U1032 is another eight bit register that retains data written at address 1F. Only seven sections of U1032 and U2032 are used (DB0-DB7), DB0 is routed through UI3038C. These registers are responsible for storing the microcomputer's latest command and controlling most of the operation of the sweep board.

Commands that can be written at address 0F are: 1) sweep start for single sweep mode (bit 0 high); 2) internal frequency reference on or off (bit 1 low for on and high for off); 3) single sweep operation (bit 2 high); 4) sweep rate selection (bits 3-7, see Table 7-11)

TABLE 7-11
SWEEP RATE SELECTION CODES

Sweep Rate	D7	D6	D5	D4	D3
20 μs/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

Commands written to address 1F control the triggers and sweep holdoff time.These commands are as follows: 1) abort sweep without starting another in the single sweep mode (bit 0 goes high); 2) ignore input trigger signals (bit 1 high); 3) disable sweep gate and blank non-store display (bit 2 high); 4) trigger mode (controlled by bits 3 & 4, see Table 7-12; 5) sweep holdoff time (bits 5 & 6, see Table 7-13; 6) interrupt at end of sweep (bit 7 goes high).

Table 7-12

TRIGGER MODE	D4	D3
Free run	0	0
Internal	0	1
External	1	0
Line	1	1

Table 7-13

SWEEP HOLDOFF	D6	D5
Short	0	0
Medium	0	1
Long	1	0

Address 9F reads the Frequency Reference Lock module status. An interrupt is generated when a change in status of the reference lock occurs. When the internal reference frequency is in use, bit 0 is high. When an external reference is used, the bit goes low. When the 100 MHz, 3rd LO, is locked to the frequency reference, bit 1 is high; and conversely, if the bit is low the 3rd LO is not locked.

The sweep board consists of five major circuits: 1) the sweep generator, which generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage, the Preselector, and the swept oscillators; 2) the trigger circuits, which process and multiplex the three trigger signals; 3) the sweep control circuit, which generates the SWEEP GATE and PEN LIFT signals and determines the holdoff time for the sweep generator; 4) the digital control circuits, which receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, select internal or external reference frequency, and control interrupts to the microcomputer; 5) the interface between the microcomputer and the Reference Lock module.

The analog section of the Sweep board consists of, the ramp or sweep generator plus its output buffers that drive

the deflection amplifiers, the oscillators, digital storage, Z axis, and the trigger circuits. The sweep and trigger circuits are digitally controlled.

The Sweep Generator

The sweep generator is an integrator circuit consisting of operational amplifier U2062 with one fixed and two selectable capacitors in the feedback circuit. The fixed capacitor (C1061) is used for the faster sweep rates. The other two capacitors (C1065 or C1062)are added, to change the time constant, when either Q1061 or Q1058 are switched on by compartors in U3054.These comparators are driven by register U2032, which interfaces to the instrument bus. For manual sweep operation, Q1064 is turned on and the integrator (U2062) becomes an amplifier.

Timing resistors are connected between a −12 V reference, out of U3059B, and the input to the integrator U2062 by multiplexer U3064. Data bits D5, D6, and D7 of address OF drive the select inputs of the multiplexer. The voltage reference of −10 V out of U2061 is boosted to −12 V by U3059B. A voltage divider (R2065, R2063) sets the noninverting input of U2062 to −8 V and feedback sets the inverting input to the same potential. Therefore a difference of about 4 volts exists across the timing resistors. The timing current through the resistors varies over two decades such that 1/I is proportional to a 2-5-10 sequence by U2061.

Switching in feedback capacitors C1061, C1065, and C1062, changes the sweep rate 100 times. Sweep Accuracy adjustment (R1063) compensates for differences in timing voltage or timing circuit values. The timing capacitors are matched so one adjustment compensates for small variations in each set.

Trigger Circuits:

The sweep circuit can be triggered by; an externally applied signal, the internal video, or from the line. Each trigger signal is converted to TTL level before it is applied to the trigger multiplexer which is part of the trigger control circuit. The trigger control circuit selects the desired triggering signal and triggering mode or rejects the trigger so the sweep circuit free runs, is manually controlled or the external sweep mode is used.

An external trigger signal, that is applied to the external HORIZ/TRIG connector, is converted to TTL level by Q1052. CR1046 and CR1044 limit any voltage surges that may be on the line. Line trigger signals, from the power supply, are filtered by R1026 and C1039 then applied through comparator amplifier U1015C to the multiplexer. Video signals from the Video Processor are buffered by Q1051 and converted to TTL level by Q1053. Both the external and video trigger signals are applied to multiplexer U2026, through a Schmitt trigger inverter in U1037.

Under control of the data (D3,D4) out of register U1032, the multiplexer selects the trigger signal and passes it to flip-flop U1026B. After retrace and holdoff time, U1026B allows a trigger to pass through U2026 and U2015C to reset the Sweep State Control flip-flop U3021. When U3021 is reset the integrator starts a new sweep.

Sweep Output Circuits

The sweep ramp from the integrator is applied through buffer amplifiers, U3042 and U3048, and a bus on the Mother board to: the Deflection Amplifiers, Span Attenuator, and Digital Storage board. The sweep out of U3042 is an 11 V peak-to-peak ramp centered around 0 V. The sweep out of U3048 is a 22 V peak-to-peak ramp for the oscillator.

The sweep signal also drives a pen-lift comparator U1015B, and the end-of-sweep comparator U1015A. The threshold for the pen-lift comparator is +7.4 V. The threshold for the end-of-sweep comparator is +8 V. The sweep ramp, from the integrator, starts at −8 V and rises towards + 8 V. When the signal reaches +7.4 V, the pen lift comparator toggles.This output is gated through U3015B and the pen lift signal goes high. When the sweep ramp reaches +8 V, the end-of-sweep comparator, U1015A, toggles. The resultant low output is applied through U1037A to become the EOS (end-of-sweep) signal.

Sweep Control Algorithm

U3021 is the Sweep State Control flip-flop. When reset, the high at the $\overline{Q}$ output turns the FET Q1062 off and allows the integrator capacitors to charge. When the Sweep State Control flip-flop (U3021) is set, by a low on pin 4, its $\overline{Q}$ goes low. This switches the output of comparator U3054B so its output turns Q1062 on and discharges the timing capacitors. The $\overline{Q}$ output of U3021 connects to pin 5 of U2021A so this low switches the output pin 6 to its high impendance state (its output is open collector). The Q output of U3021 is high. Both U1026A and U1026B where previously set when the Q output was low. This starts the holdoff cycle or retrace time which is described detail further on.

The Sweep State Control flip-flop U3021, is set by a low out of NOR gate U2015A when either the EOS (end-of-sweep) or the ABORT SWEEP lines go high. ABORT SWEEP is generated when a 1 is written to D0 that is coincident with address 1F. The Sweep Control flip-flop is reset by either a trigger signal from multiplexer U2026 or a high on the MNL or EXT SWP line. The microcomputer writes to

bits 5 and 6 at address OF for the manual or external sweep mode.

Trigger Control Algorithm

A sweep is initiated by the microcomputer, in single sweep or manual mode as noted above, or by one of three trigger signals selected by the multiplexer U2026. Data bits D4 and D3, at address 1F (see Table 7-12) select the input trigger signals and route them to the clock input of U1026B. During sweep time the flip-flop U1026B is set by a low on the Q output of U3021.

The high on the $\overline{Q}$ output of U3021 is also applied through an inverter buffer, in U2021A, and the resultant low out discharges the holdoff capacitor C1018, at the input to U1015D. The output of U1015D is low so the output of NAND gate U1038D is high. The multiplexer U2026 requires a high-to-low transistion to clock any input through. Since it is high, incoming trigger signals will have no effect on the circuit.

At the end of sweep, the $\overline{Q}$ output of U3021 goes low. This switches the output of U2021A to its high impedance state and the holdoff capacitor, C1018, starts to charge towards +15 V through R1020. When it reaches +5 V the comparator output switches high. This, along with a high on pin 13 of NAND gate U1038D, causes the output to go low and the high-to-low transistion clocks U2026 so the incoming trigger signal can now clock U1026B and produce a high at the $\overline{Q}$ output. This is gated through U2026 to the input of U2015C, so the output of the NOR gate will now reset the Sweep Control flip-flop, U3021, and start a new sweep.

In the free-run mode the multiplexer U2026, selects the −5 V on pin 6. This high is clocked through to the Sweep State Control flip-flop immediately after retrace. Incoming trigger signals are ignored and the sweep runs in an astable mode. The microcomputer writes a "1" to bit 1 at address 1F. This is inverted by the buffer in U2021 and pulls the input to NAND gate U1038D. low which disables the multiplexer U2026.

In single sweep mode the sweep circuit cannot be retriggered until it is armed by the microcomputer. A "1" is written into bit 2 at address 0F. This appears as a high on pin 2 of U3015A. Since U1026A has been set by the previous sweep, the two highs at the input produce a low at pin 13 of U1038D. Incoming triggers therefore, are disabled. The sweep is now in an idle state and can not run until the microcomputer "arms" the trigger circuit again. This is done by writing a "1" to address 0F which produces a high out of U3038C and clocks flip-flop U1026A. The resultant low at pin 1 of U3015A forces a high at pin 11 of U1038D, and arms the trigger circuit. Thus a signal can now trigger the sweep circuit and the single sweep cycle repeats.

Sweep Holdoff

During retrace, the sweep must be held off long enough for the timing capacitors in the integrator to discharge and the circuit to stabilize. To prevent flicker, the holdoff period must vary as sweep time changes. U1015E and three selectable timing capacitors (C1018, C2022, and C2023) plus a resistor (R1020) form the holdoff circuit.

During sweep time pin 5 of U2021A is high. This pulls pin 6 low and discharges C1018. During retrace, pin 6 is released and the timing capacitors start to charge. When they reach +5 V, compartor U1015E toggles and its output goes high. This, along with the high on pin 13 of the NAND gate U1038D, provides the clock pulse for U2026 to pass a trigger signal through to the Sweep State Control, U3021.

Interface Circuits

In addition to the sweep circuits, there are circuits that interface between the microcomputer and the Reference Lock module. These circuits; generate an interrupt (SER REQ) when a change of status in the Reference Lock module occurs, respond to the POLL routine, and provide data so the microcomputer can monitor the status of the Reference Lock module.

To determine the status of the Reference Lock module, the microcomputer reads the status of bits 0 and 1 (DB0 & DB1) of the data bus . These two bits connect, through tri-state buffers U1042A and U1042D, to the INTL REF and $\overline{\text{REF LOCK}}$ lines from the Reference Lock module. INTL REF line is high when the internal reference is used and low for external reference. $\overline{\text{REF LOCK}}$ goes high when the 3rd LO is not locked to the frequency reference and low when it is locked. The buffers in U1042D are enabled when address 9F is read.

At the time a read is done, U2043 is enabled and latches the input data. Thus, the bits on pins 1, 2, and 5, 6, of the exclusive-nor gates on U1048 match each other. The open-collector outputs are wired together, so when the outputs are high, inverter U2021B applies a low to the clock input of flip-flop U2048A. When a change in status occurs, one of the bits to the exclusive-nor gates (pin 1 or pin 5) changes. There is now a difference between the present status and the previous status, stored in U2043. One output of U1048 now outputs a "0" and a low-to-high transition occurs on the clock pin of U2048A. This triggers an interrupt and causes the microcomputer to inquire about the new status. Reading the new status, activates the latch and resets the circuit. Transistor Q2038, driven by bit 1 at address 0, turns the INTL REF (internal reference) on or off. When "0" is written at address OF, the status of data bit 1 turns the frequency reference off or on.

U2048 is part of a circuit that generates the instrument bus interrupts and responds to the subsequent poll routine from the microcomputer. There are two sources of an interrupt from the sweep board, either an EOS (end-of- sweep) has occurred or a change of status of the reference lock module has occurred. When an EOS occurs, and provided the EOS Interrupt Enable bit is high, the flip-flop U1022A is clocked and its $\overline{Q}$ goes low. This produces a high out of U1038B which turns Q2036 on to pull the instrument bus line SER REQ (service request) low and forces an interrupt.

The microcomputer response to an interrupt is with a poll routine. It first writes "FF" to the instrument address bus. None of the decoders respond, but bit 7 of the address bus (AB7) goes high. The microcomputer raises the POLL line and reads the instrument data bus. The output of U3038A goes low. This, anded with the low out of U1022A, generates a high to turn Q2034 on and pull bit 4, of the instrument bus, low. When the microcomputer reads a low on bit 4 it lowers the POLL line and writes 7F on the instrument bus. None of the decoders respond, however, bit 7 (AB7) of the address is pulled low. The microcomputer now writes a word to the data bus with all bits except 4 high. This acknowledges the interrupt. The microcomputer now raises the POLL line and, since both inputs to U3038B are high, the output of the gate goes low. The POLL line is then pulled low and the low-to-high transition clocks the low on the D input of U1022B through to reset U1022A. Its Q output then sets U1022B. Q2036 is cut off, the interrupt is removed, and the circuit is now ready for another EOS.

When a change-of-status occurs, in the reference lock module, a low-to-high transition occurs on the clock input of U2048A to latch the Q (pin 5) output high and the $\overline{Q}$ output low.This low is gated through U1038B to turn Q2036 on, and pull SER REQ line low. When the microcomputer responds, by writing "FF" and raising the POLL line, U3038A output goes low, however, at this time U2015B output goes high, because of the low on pin 6 of U2048A-6. This turns Q2018 on and bit 6 on the data bus goes low. The microcomputer reads this and pulls the POLL line low. Address "7F" is written on the address bus and the POLL line is raised. This forces U3038B to output a low and the POLL line again goes low to toggle U2048B. The low output at Q resets U2048A to remove the interrupt or SER REQ. At the same time U2048B is reset and the circuit is ready to repeat the sequence.

SPAN ATTENUATOR 

The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 32 as well as the schematic diagram. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver and Preselector Driver circuits; and the decade attenuator, which provides three decades of attenuation for the output signals.

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal. Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are cancelled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either increase or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting, under bus control. When line Q8 of latch U2015 is low, Q2023 conducts and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3028 to the summing node of the amplifier, and the gain of the stage is −1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly −15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042, amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 7-23 illustrates a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the summing node of the amplifier is at ground potential, the magnitude of the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2^2 or 4 output values possible. In the actual 10-bit converter, there are 2^{10} or 1024 output values ranging from 0 to 1023/1024 of the input.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the V_{ref} input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062/Q3056. The pair is biased to produce a standing current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

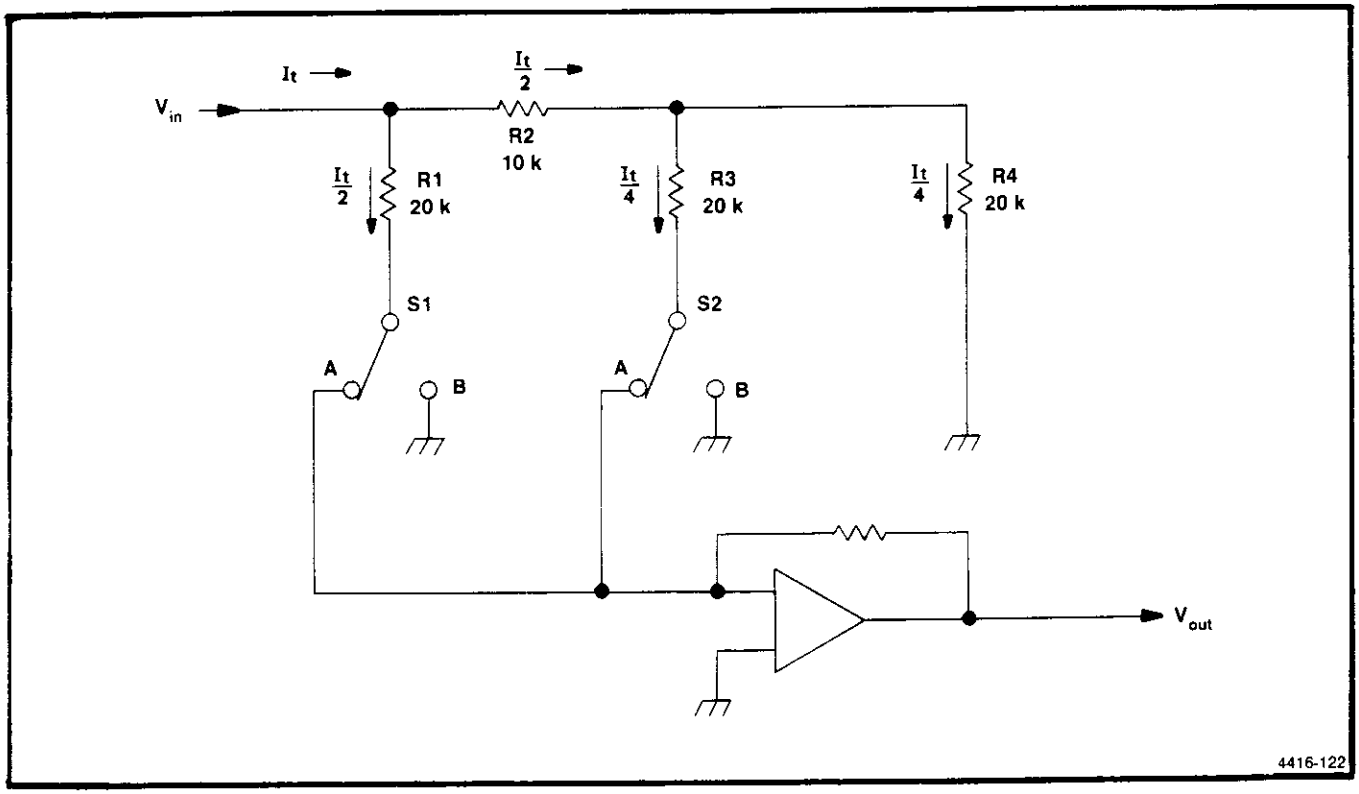


Figure 7-23. Simplified digital-to-analog converter (DAC).

One-of-four decoder, U4025, uses data bits DB3 and DB4 lines from U2015, to control three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 7-14 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 7-14
CALIBRATION CONTROL SELECTION CODES

U4025		
DB 3 (Pin 3)	DB4 (Pin 2)	Selected Adjustment
0	0	R1065 (main coil)
0	1	R1071 (FM coil)
1	0	R1067 (2nd LO)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1, and X1 (see Figure 7-24 for a simplified circuit diagram).

The "2" side of U4025 is controlled by data bits, DB5 and DB6,on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffers in U4042 to select the appropriate attenuation factor for the output sweep. Table 7-15 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transients.

Table 7-15
ATTENUATION SELECTION CODES

U2015		
Pin 15 DB5	Pin 16 DB6	Attenuation Factor
0	0	X1 (K3065)
1	0	X 0.1 (K3075)
0	1	X 0.01 (K4072)

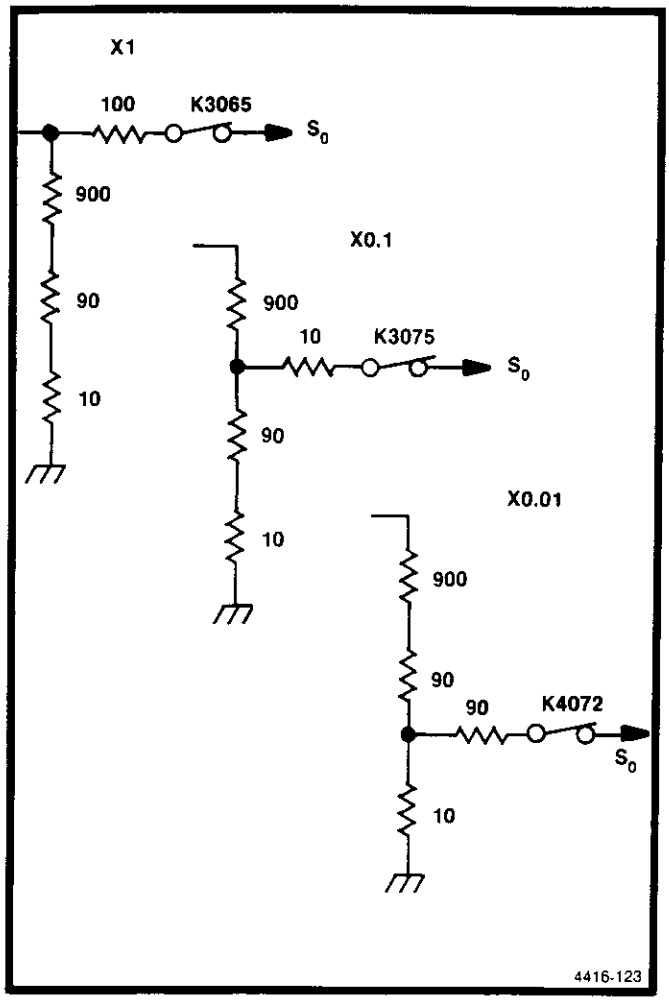


Figure 7-24. Simplified span decade attenuator.

1st LOCAL OSCILLATOR DRIVER 33

The 1st LO Driver performs the following functions: 1) Buffers the TUNE VOLTS signal and applies it to the dot marker circuit; 2) combines the SPAN VOLTS with the COARSE TUNE VOLTS and outputs the combination to the Preselector Driver (the combined signal is also applied to the Oscillator Driver circuits, which drive the 1st Local Oscillator coil); 3) selects and outputs the appropriate bias voltage to the internal or external 1st Mixer; 4) outputs a voltage to the Preselector Driver that peaks the Preselector; 5) controls the oscillator filter switch; 6) produces a stable and precise −10 V reference for both the 1st LO Driver and the Preselector Driver circuits.

The major circuits and their function are as follows:

1. The digital control circuits buffer the incoming data from the data bus, decode the address data, select the required mixer bias, connect or disconnect the TUNE VOLTS and SPAN VOLTS signals to the summing amplifier, energize the filter switch in the 1st LO assembly, and control the drive and filtering of the oscillator driver stage.

2. The tune volts buffer buffers the COARSE TUNE VOLTS signal between the Center Frequency Control and the dot marker circuit on the Crt Readout board. It also reduces the signal amplitude to drive the dot marker circuits.

3. The oscillator filter switch driver furnishes drive current to the capacitor switching relay in the 1st LO assembly.

4. The input switching circuit connects or disconnects the SPAN VOLTS and COARSE TUNE VOLTS signals to the input of the summing amplifier.

5. The summing amplifier furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal, from the Span Attenuator, with the COARSE TUNE voltage, from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ±10 V sweeps the oscillator at a rate of 333 MHz/division. As the TUNE VOLTS signal varies from −10 to +10 V, the oscillator's center frequency is moved over its full range.

6. The oscillator driver furnishes the current drive for the 1st LO coil.

7. The −10 V reference supply produces a precise −10 V reference for the 1st LO Driver and the Preselector Driver.

8. The mixer bias circuit produces and outputs the required bias voltages for the 1st Mixer.

9. The programmable bias circuit provides peaking voltage for the Preselector or external mixers bias voltage based on data supplied by the microcomputer.

Digital Control

The digital control circuit sets the oscillator span volts, the 1st Mixer bias and programmable bias for the 494P. Decoder U4034 output Y1 (pin 14) goes low when the input address is 72 and output Y7 goes low for address 7E. When output Y1 goes high, data is clocked or latched into U4017, and when Y7 goes high data is latched into U4024 and U4022.

Data for U4017 consists of control codes for the oscillator drive circuits and the switches in U1016, which select 1st Mixer bias or the bias set by the front panel MANUAL PEAKING control. The codes are described where each applies to the description and in Table 7-16. Data for DAC U3022 is converted to an analog signal which provides the Programmable Bias for the instrument.

Tune Volts Buffer. The tune volts buffer consists of amplifier U1025B and surrounding components. The COARSE TUNE VOLTS signal, from the Center Frequency Control circuits, is divided down by R1028,R1027, and applied through a unity-gain amplifier, U1025B, to the dot marker stage in the Crt Readout circuits.

Table 7-16
U4017 OUTPUT LINES

	Low	High
Q1(DB0)	Bias 1 connected	Bias 1 disconnected
Q2(DB1)	Bias 2 connected	Bias 2 disconnected
Q3(DB2)	Bias 3 connected	Bias 3 disconnected
Q4(DB3)	Manual peaking connected	Peaking disconnected
Q5(DB4)	Driver filter disconnected	Driver filter connected
Q6(DB5)	Driver input connected	Driver input disconnected
Q7(DB6)	SPAN VOLTS line disconnected, oscillator filter connected	SPAN VOLTS line connected, oscillator filter disconnected
Q8(DB7)	Maximum span; TUNE VOLTS line disconnected	Normal span; TUNE VOLTS line connected

Input Switching. This stage consists of FET Q2033, comparators U3014A and U3014C, and FET Q2026. When maximum span is selected, line Q8 of U4017 goes low, causing U3014C to switch. This turns Q2026 on and shunts R2031 with R2030, increasing the stage gain of U2032. This low is also applied to the comparator U3014A, which switches and cuts off Q2033. This disconnects the TUNE VOLTS signal to the summing amplifier U2032; the TUNE VOLTS is now used to position a marker on the display at the center frequency. The span voltage sweeps the oscillator over its full frequency range.

If the main coil of the oscillator is not to be swept, DB6 (line Q7 of U4017) goes low. This cuts Q3028 off, de-energizes K3034 and disconnects the SPAN VOLTS signal to the summing amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Switch Driver. When relay K3034 is deenergized, DB6 is low, Q2029 is biased on which drives a capacitor-switching relay on the 1st LO Interface board. The capacitors are switched across the main coil, when it is not being swept, to filter noise riding on the tuning current. Capacitor C2025 provides a gradual decay of current through the relay after power is turned off.

Summing Amplifier. Amplifer U2032 and the complementary pair of transistors, Q2035 and Q2039, plus related components, comprise an operational amplifier. The COURSE TUNE VOLTS and the SPAN VOLTS are summed at the input to U2032. The feedback resistor, for the operational amplifier, is R1038.The input resistance is R2027 for the COARSE TUNE VOLTS signal and R2031 for the SPAN VOLTS signals. (R2030 is switched across R2031, as mentioned previously,to increase stage gain for maximum span operation.) The output of the summing amplifier, which can swing from −10 V to +10 V, is applied to the Preselector Driver circuits and to the Video Processor board.

Oscillator Driver. The output of the summing amplifier also drives the input to the oscillator driver stage when FET Q2040 is switched on. The oscillator driver stage consists of active components Q2045, U2043, Q3047, and Q352. The input resistance consists of R2041, the 1st LO Sensitivity adjustment R1031, plus R2043. The feedback resistance is R2042. The amplifier converts a voltage input into a current drive for the 1st LO tuning coil by controlling the voltage across current sense resistor R1040, which is in series with the oscillator tune coil. Q3047 assures that Q352 base current remains within the oscillator tuning coil circuit. Q2040 is biased on except when the oscillator is degaussed. The output of the operational amplifier U2032, Q2039 and Q2035, is applied through the 1st LO Sensitivity adjustment R1031, and summed with an offset voltage set by the 1st LO Offset adjustment R1032, at the input to the preamplifier stage Q2045. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. R1032 adds offset to the input of the preamplifier to place the oscillator at center operating frequency when the amplifier input is at zero volts.

Q2045 is a low-noise, matched, dual transistor. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage sets the current through the resistor which is also emitter current for driver transistor Q352. The 1st LO Sensitivity adjustment R1031, sets the voltage gain of the amplifier. This in turn, changes the current drive to the oscillator coil.

Capacitor C3038 lowers the noise bandwidth of the output amplifier when it is switched into the circuit by Q3042. Because of its effect on the tuning rate of the 1st LO, the capacitor is only in the circuit in phase locked spans with the ϕ Lock switch off (other than 494/494P spectrum Analyzers). Since the 494/494P control system does not allow the phase lock to be turned off, DB4 is held low and Q3042 is biased off, effectively removing C3038 from the circuit.

Reference Supply. Preamplifier Q2052 plus amplifier U2052 and emitter follower Q2051, are the active components of the −10 V reference supply. Bias for one side of Q2052 is set by VR1055 . The other side is set by the −10 V Ad. R1034. Any change in the supply is amplified by Q2052 which changes the drive to the pass transistor Q2051 which compensates for the change.The diode network across the base-emitter junction limits the emitter current to about 30 mA, protecting the transistor from damage.

Mixer Bias Driver. The mixer bias driver circuit, which consists of quad FET switch U1016, amplifier U1025A, and buffer Q2025/Q1028, plus associated circuitry, furnishes the required bias current (up to 20 mA) to the 1st Mixer circuit. The bias voltage varies from +1 V to −1 V for the internal mixer, and from +1 V to −2.25 V for an external mixer. External mixer bias voltage range can be changed to −1 to +2.25 V by moving the strap J2014 from +12 V to the −12 V supply.

Mixer bias is selected, by the data out of U4017 to the quad FET switch U1016, and fed to the inverting input of U1025A. The output of U1025A drives the base of a pair of complementary transistors Q1028 and Q2025 which provide the 1st Mixer Bias voltage. When any of the Q1 through Q4 (D0 to D3) lines of U4017 go low, the respective switch within U1016 closes and connects one of the Bias adjustment potentiometers or the output of U2018 (the programmable bias line) to the input of U1025A.

When the Q4 (DB3) line of U4017 goes low, U1016 selects the Programmable Bias line as the 1st Mixer Bias source. This occurs when External Mixer mode is selected. The Programmable Bias is set by the data loaded into DAC U3022, by the microcomputer, or by the front panel MANUAL PEAK control. The MANUAL PEAK control is connected to the input of U2018 when the Q5 line (DB4)of U4024 goes low and turns Q3019 on. When MANUAL PEAK is selected, the DAC output is set for 0 V.

Programmable Bias. When the microcomputer sends address 7E to decoder U4034, pin 7 (output Y7) goes low. At the end of data output cycle, data is clocked into either U4024 or U4022, depending on which latch is enabled by DB6 or DB7. This data is then converted to an analog current by U3022 which is the current source for operational amplifier U2018. The resistance between output terminals 16, 2, and 15 of U3022 is the input resistance for operational amplifier U2018. R2022 is the feedback resistance. The output of U2018 is a bias voltage that is fed, via the Programmable Bias line, to either the Preselector Driver board where it is summed with the drive voltage for the Preselector; or, it is fed through U1016/U1025A, and Q1025/Q2025 to the 829 MHz Diplexer, then through the Transfer Switch on the RF deck to the External Mixer port.

Oscillator Collector Supply. This circuit comprises amplifier U4055, buffer Q3049, and surrounding circuitry. U4055 holds Q3049 in saturation, so the collector of the transistor remains at a fraction of a volt below +15 V. This voltage is applied to the 1st LO collector.

PRESELECTOR DRIVER 

The Preselector provides RF input selectivity between 1.7 and 21 GHz.This selectivity reduces spurious responses over this frequency range. Refer to the block diagram adjacent to Diagram 34 as well as the schematic. The Preselector Driver supplies the drive current to the Preselector coil, depicted on Diagram 12, to tune the Preselector. It also furnishes a voltage that is proportional to frequency change through the rear-panel ACCESSORIES connector for an external preselector, if used. The circuit also operates the filter select relay that selects either the Preselector or Low-pass Filter. The major circuits and their function are as follows:

1. The digital control circuit, which stores and decodes the data from the microcomputer and controls the other circuits within the Preselector Driver. The digital control circuit; applies the SPAN VOLTS signal to the oscillator voltage processor when FM coil spans are selected, selects the gain of the oscillator voltage processor, turns off the drive signal to the current driver for degauss cycles or when the preselector is not in use, selects the IF offset voltages to be combined with the FINE TUNE VOLTS signal, adds noise filtering at the driver output when the preselector is not being swept, and controls the filter select switch;

2. The oscillator voltage processor, which attenuates and offsets the input signal for application to the summing amplifier.

3. The IF offset stage, which applies an offset voltage to the summing amplifier. This offset is proportional to the 1st IF frequency in use, including the effects of fine tuning frequency changes of the 2nd Local Oscillator.

4. The summing amplifier, which combines the effective oscillator frequency voltage and the IF Offset voltage to drive the tracking adjustment circuits.

5. The tracking adjustment circuit, which compensates for different preselector sensitivities, compensates any preselector offset, and compensates for non-linear operation caused by magnetic saturation of the Preselector.

6. The final driver stage, which changes the applied signal voltage into a current drive for the Preselector coil.

7. The preselector switch driver, which drives the filter select switch, depicted on Diagram 12. The switch requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

Digital Control Circuits

The microcomputer interface circuits, which exercise digital control of the Preselector Driver circuits, consist of address decoder U5036 and latch U5031. Both the write address (77) and the read address (F7) are decoded by U5036.

Data is latched into U5031 on the trailing edge of the DATA VALID signal for address 77. This event coincides with the rising edge of the pulse on pin 3 of U5036. Table 7-17 lists output lines from U5031.

In some 49X series instruments, the read address function is used by the microcomputer to determine if the instrument is equipped with an option that includes the Preselector. The Preselector is installed in all versions of the 494/494P. When address F7 is specified, the Y7 line of U5036 goes low. This pulls data line D4 low, informing the microcomputer that a Preselector is used.

Table 7-17
U5031 OUTPUT LINES

	High	Low
Q1(DB0)	Selects X1 gain for U2028.	Selects X3 gain for U2028.
Q2(DB1)	Not used.	Not used.
Q3(DB2)	Connects tracking adjustment output to final driver stage.	Disconnects tracking adjustment output from final driver stage. (Preselector current goes to zero.)
Q4(DB3)	Connects SPAN VOLTS signal to U1011A input for FM coil spans.	Disconnect SPAN VOLTS from U1011A.
Q5(DB4)	Selects Low-pass Filter (Band 1).	Selects Preselector (Bands 2-5).
Q6(DB5)	Disconnects output filtering.	Adds output filtering.
Q7(DB6)	Connects −829 MHz offset.	Disconnects −829 MHz offset.
Q8(DB7)	Connects +829 MHz offset.	Disconnects +829 MHz offset.

Oscillator Voltage Processor

The oscillator voltage processor consists of U1011A, U2028, and related components. The Preselector Drive signal from the 1st LO Driver is applied to a voltage divider and scaling network consisting of R1022, R1023, R1024, and Input Offset adjustment R1031. The input voltage is ±10 V. This voltage is the summation of the sweep and tune voltages, with appropriate scaling. The output of the voltage processor is about 1 V at 2.072 GHz to about 3 V at 6.35 GHz, which corresponds to a scale factor of 2.1 GHz/volt. The voltage is directly proportional to frequency; thus the offset is such that if the oscillator could operate to 0 Hz, the voltage processor output would be at 0 V.

Since the preselector drive input is not swept by the 1st LO Driver, when FM Coil spans are used, the SPAN VOLTS,from the Span Attenuator, must be summed by this stage. Line DB3 (Q4 of U5031) goes low when FM coil spans are selected, which turns Q1011 on. This switches the FET Q1022 on so the Span Volts signal is now applied to the inverting input of U1011A, where it is inverted and applied to the input of U2028.

Operational amplifier U2028, has a gain of 1 or 3, as directed by the microcomputer. The output signal in the X3 gain mode represents the effective oscillator frequency swing for bands 4 and 5 when the 3rd harmonic of the LO is used. When the DB0 (Q1 line of U5031) goes low, the respective output of quad comparator U5022 is also low, which holds FET Q2024 cut off. U2028 is now a unity-gain, non-inverting amplifier. When the DB0 goes high, Q2024 switches on and the gain of U2028 is a factor of three. The X3 Gain adjustment, R1052, sets the gain to precisely three in the tripler mode.

IF Offset

The −10 V reference, from the oscillator driver, furnishes the precise reference voltage for the IF offset circuit. Since the offset voltage is proportional to the IF −2.072 GHz, no offset is required for the +2.072 GHz IF. FET Q2034 adds the +829 MHz network into the circuit and Q2036 adds the −829 MHz network. DB6 and DB7 (Q7,Q8 of U5031) through two comparators in U5022, control the two FET switches Q2034, Q2036. One, but not both, transistors are switched on to provide the offset voltage to the inverting input of U2045. An output voltage of −9 V from the amplifier corresponds to (−829 MHz) −2072 MHz or −2901 MHz.

The signal on the FINE TUNE VOLTS line, from the Center Frequency Control board, which is used to tune the 2nd Local Oscillator, is applied to the input of U2047.Since it is applied here,it is independent of the voltage tripling action in the voltage processor circuit.The tuning voltage is also applied to the input networks of U2045 through R3044, Q2034, and R1037, Q2036. By varying the magnitude of signal in the inverting path compared to the direct path, the proper magnitude and polarity of fine tune offset for each IF is provided. Table 7-18 lists the offset voltage required for each frequency band.

Summing Amplifier

The effective oscillator frequency voltage, from U2028, and the offset IF voltage, from U2045, are applied to the inverting input of U2047. This stage drives the tracking adjustments stage and furnishes a signal for external preselector drive circuits as well. The external drive line has its own return to reduce ground loops.

Table 7-18
PRESELECTOR FREQUENCY BANDS

Band	Frequency Range	IF	Harmonic	Approximate Voltage Offset
2	1.7-5.5 GHz	−829 MHz	1st	9.0 V
3	3.0-7.1 GHz	+829 MHz	1st	3.9 V
4	5.4-18.0 GHz	−829 MHz	3rd	9.0 V
5	15.0-21.0 GHz	+2.072 GHz	3rd	0 V

Tracking and Shaper Circuits

This stage consists of gain-setting, offset, and shaping circuits. Presel Sensitivity adjustment R1065 compensates for sensitivity variations between preselectors. Presel Offset adjustment R1064 compensates for the offset in the preselector. This adjustment sets the preselector frequency to 2072 MHz when the output of U2047 is at zero volts.

The four other adjustments R1054, R1056, R1061, and R1063, are part of a shaper network. The network compensates for magnetic saturation in the Preselector, which would cause a deviation from linearity at frequencies above 14 GHz. Each shaper network is switched in by a resistive divider that, at a given frequency, provides forward-bias to the diode in the shaper to shape the current output.

The front panel MANUAL PEAK control applies a small offset through R5065 to the input of the current driver stage. This corrects for non-linearity or temperature drift in the 1st LO and Preselector.

Current Driver

This stage consists of the output stage Q565/Q5052; FETs Q3061, Q3077, and Q2074; amplifiers U2054 and U3054; and transistor Q4037. When the Preselector is not in use, DB2 goes low and turns Q2074 off to reduce the coil current to zero.

Preamplifier U2054 reduces the temperature drift of the output stage. Driver Offset adjustment, R2066 nulls the offset voltage (at which point the temperature drift is least). U2054 drives amplifier U3054. Q3061 isolates U3054 from the output driver Q5052/Q565.

Current amplifier Q5052 drives the main preselector driver transistor, Q565. The stage is biased so the current divides, with most of the current going through the output transistor, and a lesser portion through the bias circuits. The currents rejoin at the Preselector coil. One set of terminals for R4049 carries the coil current, the other set senses the voltage.

When DB5 line goes low, the Preselector is not swept, Q4037 and Q3077 turn on, which adds C4071 across the Preselector coil to reduce noise at the output.

Preselector Switch Driver

Operational amplifier U1011B and the complementary pair of transistors Q4025/Q3025, form the preselector switch driver. This circuit drives the filter select relay as is shown on Diagram 12. This relay requires a positive pulse to select the Low-pass Filter and a negative pulse to select the Preselector.

When DB4 line (Q5 of U5031) goes high, a positive pulse of about 100 ms in duration, generated through RC network C3021/R3021, is applied to the input of U1011B. The output of the operational amplifier drops to about −12 V and a positive pulse is passed through the transistor pair, selecting the Low-pass Filter. When the DB5 line goes low, a negative pulse of the same duration is passed to U1011B. The amplifier output rises to about +12 V and a negative pulse is passed through the transistor pair to select the Preselector.

When the circuit is quiescent neither Q3025 nor Q4025 conduct, since the sum of the zener voltages of VR3011 and VR3012 is greater than the combined supply voltages. When the output of the operational amplifier comes near one of the supply voltages, the transistor, that is connected to the other supply, becomes saturated, and supplies the drive current to actuate the relay coil. CR4012 and CR4013 protect the driver transistors from induced voltage surges and C3028 and R3028 dampen oscillation that occur in the coil.

CENTER FREQUENCY CONTROL ◈35

Refer to the block diagram adjacent to Diagram 35 as well as the schematic. The Center Frequency Control converts digital information, from the front panel FREQUENCY control or on the GPIB bus, via the microcomputer, to analog voltages for the 1st LO Driver and Preselector Driver.

These in turn control the center frequency of the analyzer. The Center Frequency Control board contains the following major circuits:

1. The Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits.

2. The coarse and fine storage registers (latches), which store the numerical bytes that control the DAC (digital-to-analog converter) stages.

3. The coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values.

4. The coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine and compare the stored value to the approximated value for the microcomputer.

5. The write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

An explanation of circuit design principles is given before the operation of the circuit is described. Althought DAC IC's can now furnish high resolution, two DAC IC's are used in tandem to get the required resolution for the 494/494P. This method, however, can cause errors and non-monotonic behavior in the overall converter circuit. To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits (that is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or 2E-10 bit of the high order DAC). The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

Upper order: 1 0 0 0 0 0 0 0 0 0 0 0 0
Lower order: 1 1 1 1 1 1 1 1 1 1 1 1 1

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be incremented. Thus, the two must appear as follows:

High-order: 1 0 0 0 0 0 0 0 0 0 0 0 0
Low order: 1 1 1 1 1 1 1 1 1 1 1 1 1

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete and the low-order incrementation could occur. However, the DAC device can vary by one LSB of the correct value. Figure 7-25 illustrates a graph of the best and worst case output. Note, that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.

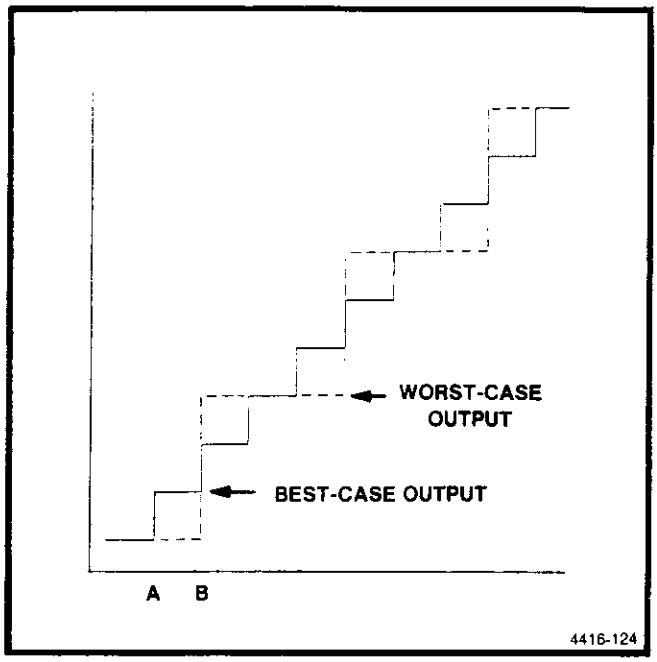


Figure 7-25. DAC variance graph.

If, in the example shown previously,the high-order device is at point A in Figure 7-25, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational amplifier. Figure 7-26 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit

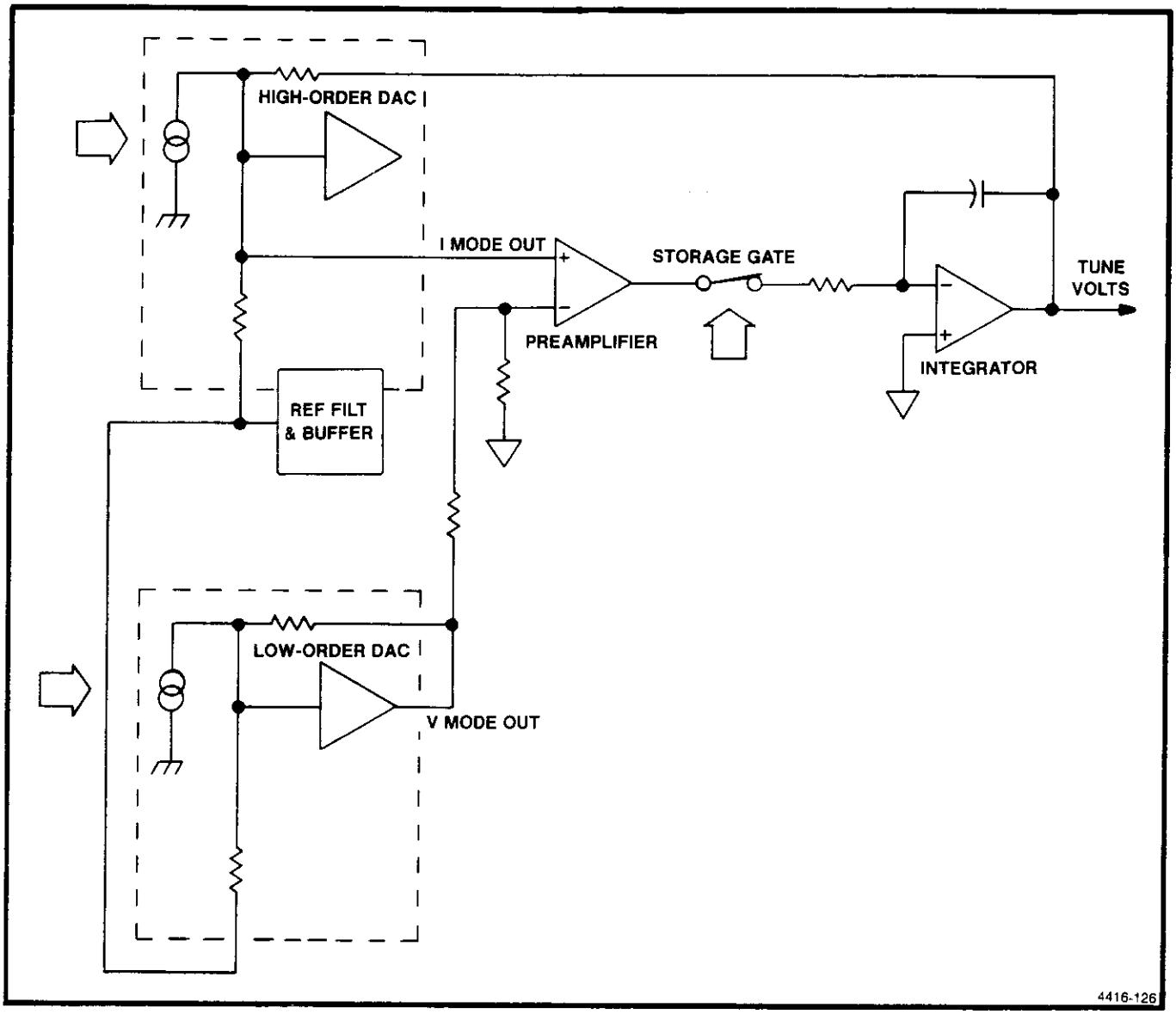


Figure 7-26. Simplified tune voltage converter.

to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signalled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

Digital Control

The digital control circuits consist of buffer U2016, address decoder U2014, steering register U2022, and the steering gates (U2024A, U2024B, U2024D, U2026A, U2026B, and U2026C). Because of the quantity of data that

must pass through these circuits, a steering register is used that has a separate address. The first byte of data, which is the steering byte, is clocked into U2022 by ADDRESS 70. The output levels are applied to the steering gates, and the circuit waits for the next byte. The microcomputer then furnishes the first byte of data to be sent to low-order, fine-tune, digital-to-analog converter (DAC); for example, via storage register U3022. The byte is clocked into the register by the coincidence of low states at the inputs of U2026C; one from the steering byte and the other from the ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the circuits, including the steering bytes. The third output from U2014, ADDRESS 80, controls transistors Q2043 and Q1039, which enable the write-back function.

In addition to the six steering lines, that drive the steering gates, U2022 also controls, by means of the $\overline{\text{TRACKf}}$ and $\overline{\text{TRACKc}}$ lines, the hold/track selector transistor for each converter side. Table 7-19 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 7-20 lists some of the significant states that are used to tune the DAC.

Table 7-19
ADDRESS 70 FORMATS

DB0	Fine Tune low byte enable
DB1	Fine Tune mid byte enable
DB2	Fine Tune high byte enable
DB3	Fine Tune hold
DB4	Coarse Tune low byte enable
DB5	Coarse Tune mid byte enable
DB6	Coarse Tune high byte enable
DB7	Coarse Tune hold

Storage Registers. Six storage registers are used in the circuit (U1014, U1016, U1022, U3014, U3016, and U3022 respectively). Since both sets are identical, only the first three are described.

Data from U2016, the data buffer, is clocked into the registers each time a different tune voltage is required. U1022 feeds the lowest eight bits to the low-order DAC, U1020; U1014 feeds the highest eight bits of the high-order DAC, U1026; and U1016 feeds the remaining bits to both units.

Digital-To-Analog Converters. Each side of the converter has two DAC stages contained on sub-assemblies A46A1 DAC 1200 Interface and A46A3 DAC 1200 Interface. These sub assemblies plug into the Center Frequency Control board, A46, through IC sockets J1024 and J1030, for the Coarse Tune circuit, and J3024 and J3030, for the Fine Tune circuit. Since both sets operate the same, only Coarse Tune units are described. Each DAC furnishes current or voltage outputs that are commensurate to the data applied. Figure 7-26 is a functional block diagram of each DAC, illustrating its operation in the circuit. U1020 is the low-order DAC, U1026 is the high-order DAC. U1012 and Q1018 and the associated circuitry are used to filter and buffer the +10 V Ref output of the high order DAC to provide the V Ref in voltage for both DAC's.

The DAC unit is basically a programmable current generator that drives an internal high quality operational amplifier. In this configuration, only the low-order DAC uses the internal operational amplifier. Thus, the low-order unit operates in the voltage output mode, and the high-order unit operates in the current output mode. The two devices feed the two inputs of preamplifier U1044, which sums the two inputs, amplifies the sum, and sends it through the switching circuit to the integrator.

Table 7-20
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's.
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DAC's. Midrange value
Negative-full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DAC's

Since the DAC units generate the dc voltage that tunes the entire instrument, noise and extraneous signals must be kept at a minimum. Thus, each tune voltage is provided with an isolated ground system, U1042A/U1042B for the Coarse Tune voltage converter, and U3041A/U3041B for the Fine Tune voltage converter.

Track/Hold Amplifiers

Since the coarse and fine amplifiers are identical in operation, only the coarse amplifier is described here. The amplifier consists of preamplifier U1044, control transistor Q2044, storage gate FET Q2046, and integrator amplifier U2046.

The output of the low-order DAC (U1020) is fed through input resistor R1048 to the inverting input of preamplifier U1044. The current output of the high-order DAC U1026, is fed directly into the non-inverting input of the preamplifier. Feedback resistor R1044 establishes the gain of the stage at about 10,000 (ratio of R1044 to R1046). The combination of CR1046, CR1045, and R1047 in the feedback circuit, prevents the output from swinging to extreme voltages with large input signals. Thus, whenever the output exceeds about one volt in either direction, one of the diodes conducts and connects R1047 and R1045 across the feedback path to reduce the gain of the stage to about unity.

The output signal from the preamplifier is connected to the source of storage gate FET Q2046. The gate of this device is controlled by transistor Q2044. Normally the circuit is tracking, so $\overline{\text{TRACKc}}$ line (Q8 of U2022) is low and Q2044 is conducting. CR2042 is cut off since the voltage drop across R2043 holds the gate of Q2046 at about 0.3 V. (The 0.3 V back bias on the source-gate junction reduces memory slewing while switching modes.) Q2044 holds the diode back-biased as long as the transistor continues to conduct. This permits Q2046 to pass the signal from the preamplifier output to the integrator input.

Integrator U2046 tracks the preamplifier output during track mode and serves as the inverting amplifier for the feedback system shown in Figure 7-26. Under normal circumstances the incoming signal is routed through R2046. To improve the amplifier's slewing rate, CR2044 and CR2045 conduct to connect R2047 in parallel with R2046 when signals in excess of one volt are applied. This speeds up the response of the circuit when large scale tuning changes are required.

When the hold mode is selected, the $\overline{\text{TRACKc}}$ line (Q8 of U2022) moves high, Q2044 cuts off and CR2044 pulls the gate of Q2046 low enough to cut off the FET. This disconnects the preamplifier from the integrator which then maintains the charge on C2046 during the approximation routine. COARSE TUNE RANGE adjustment R1032 is connected across pins 16 and 18 of U1030. It compensates for the different resistance values inside the DAC. This variation is more serious in the higher-order DAC owing to its greater effect on the output.

Write-Back Circuits

These circuits consist of amplifier U2044 and U3045, plus enabling transistors Q1039 and Q2043. Since both are identical, only the coarse circuit is described.

Following the command to shift to the hold mode, the microcomputer will interrogate the circuit to see if the DAC output and the stored voltage match. It does this by pulling $\overline{\text{ADRS 80}}$ low. This turns Q1039 off, which enables U2044. The output of U1044 is at zero volts when its two input voltages match. If the loop error voltage is high, U2044 will pull down on DB7 line, and if the loop error voltage is low U2044 will allow DB7 to go high. This informs the microcomputer whether the bit just set is too large or too small. The output of U2044 is open collector, so it has no affect on the data line when it is not disabled.

COUNTER AND PHASE LOCK SECTION

FUNCTIONAL DESCRIPTION ◈8

This section of the 494/494P consists of a Counter, Phase Lock assembly, Phase Gate, Harmonic Mixer, and Auxiliary Synthesizer. The Counter, Harmonic Mixer, and Auxiliary Synthesizer, comprise the nucleus of the frequency control hardware for the instrument. Both the 1st LO and 2nd LO frequencies are controlled via a firmware based control loop that uses data from the Counter as feedback to control oscillator frequency. The 10 MHz IF is also counted to accurately calculate signal frequency.

The Phase Lock assembly stabilizes the 1st LO frequency. It consists of an outer and inner loop. The inner loop uses the subharmonic of the 100 MHz reference frequency, from the 3rd Converter, to mix with the output from a 25.032 to 25.095 VCO and compares this IF difference with a ÷N number (between 32 and 94 kHz) set by the processor. Any deviation is detected by a phase/frequency detector whose output error voltage is used to pull the VCO frequency and phase into lock with the inner loop reference. The outer loop consists of the inner loop, a Strobe Driver, Phase Gate Detector.Error Amplifier, and the 1st LO. The frequency of the inner loop VCO is divided down and applied as a strobe pulse to the Phase Gate Detector. This strobe pulse generates a spectra of equally spaced line spectra across the spectrum. One of these lines will be within 2.5 MHz of the 1st LO frequency (the other input to the Phase Gate Detector). The Phase Gate Detector outputs an error signal that is proportional to the difference between the nearest strobe and the 1st LO frequency. This error signal is amplified and filtered by the Error Amplifier and applied to the FM coil of the 1st LO to pull it into frequency and phase lock with the strobe.

The Harmonic Mixer mixes the 1st LO frequency and a harmonic of a synthesized 200-220 MHz signal from the Auxiliary Synthesizer. The exact frequency of the signal from the synthesizer is a function of the ÷N factor from the processor. The output of the Harmonic Mixer is a signal within the 10 to 80 MHz range. This signal is divided down in the Auxiliary Synthesizer and sent to the Counter. The microcomputer looks at the resultant count and determines which direction to move the 1st LO to bring it to frequency.

Phase Lock Assembly

As previously stated, the phase lock system consists of two frequency servo loops, called the outer loop and inner loop. In the inner loop operation, the 100 MHz reference signal from the 3rd Converter, is divided down to 25 MHz, on the Synthesizer board, and applied as the reference signal to the mixer on the Offset Mixer board. The 25 MHz signal is also applied as a clock signal to ÷N counter circuits, on the Synthesizer board, which output a frequency (depending on the ÷N number from the processor) between 32 kHz and 94 kHz. This signal is applied to the phase/frequency detector on the Offset Mixer board, where it is compared to the IF output (difference between the 25 MHz reference and the output from the VCO (voltage controlled oscillator) and any difference is output as an error voltage to the Error Amplifier.

The VCO operates between 25.032 MHz and 25.094 MHz,depending on the drive from the Error Amplifier. This signal is applied to the RF input of the mixer on the Offset Mixer board, where it mixes with the 25 MHz reference frequency. The difference frequency, which is between 32 kHz and 94 kHz, is applied to the phase/frequency detector and compared to the ÷N frequency. If the two signals are edge and frequency coincident, phase lock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the VCO to shift the oscillator frequency until it is phase locked. This evolution typically lasts for only a few milliseconds, so the inner loop phase lock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and VCO) consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The Harmonic Mixer, Auxiliary Synthesizer, and Counter, are a part of the operation, but are not considered a part of the loop.)

The signal between 25.032 MHz and 25.094 MHz from the VCO is applied to the Strobe Driver where it is divided by five, filtered, and sent to the Phase Gate Detector as a strobe signal between 5.006 MHz and 5.019 MHz. This strobe generates line spectra that are equally spaced approximately 5 MHz over the spectrum. At about the 400th line, which corresponds to approximately 2 GHz, assuming that the 1st LO is tuned to a frequency near 2 GHz, one of these lines (at about the 400th line) will be within 2.5 MHz of the 1st LO frequency. The Phase Gate Detector will then output an error signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line, if that difference frequency is less than approximately 1 MHz.

For phase-lock acquisition, the microcomputer calculates the strobe frequency required for the desired 1st LO frequency. The strobe is set to this frequency and the 1st LO is set to the required harmonic of the strobe. The outer loop is

closed, and the microcomputer tunes the 1st LO frequency through the following sequence; up 750 kHz, down 1.5 MHz, up 1.5 MHz, and down 750 kHz. During one of these "firmware searches" the 1st LO frequency passes through the strobe harmonic frequency and the loop acquires lock.

Any frequency difference between the strobe signal and the 1st LO will generate a low frequency correction voltage. This correction voltage is filtered by the F(s) amplifier, then used to drive the oscillator FM coil to pull the oscillator frequency back to the strobe position. If the 1st LO drifts beyond the error voltage range of the F(s) amplifier, comparators on the Error Amplifier board, that monitor the error voltage, will interrupt the microcomputer and indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phase lock loop.

Frequency Control

The 21-bit counter and its associated control circuitry, on the Counter board, plus the Harmonic Mixer and Auxiliary Synthesizer, comprise the frequency control hardware nucleus for the 494/494P. A firmware-based control loop, that uses data from the counter as feedback on the oscillator frequency, controls both the 1st LO and the 2nd LO frequencies. The 10 MHz IF is also counted by the Counter to determine the input signal frequency to the analyzer.

A mix down counting scheme is used to count the 1st LO frequency, which varies between 2 GHz and 6 GHz. The 200-220 MHz output from the Auxiliary Synthesizer is positioned so one of the signal harmonics is approximately 45 MHz above the 1st LO frequency. This output drives the LO input to the Harmonic Mixer, the 1st LO drives the RF input. One of the IF outputs from the Harmonic Mixer is within the 10 to 80 MHz range (approximately 45 MHz).This IF signal is passed through a 10-80 MHz band-pass filter,divided by 100, then counted by the Counter . Since the Processor knows the Synthesizer frequency, the 1st LO frequency can be calculated if the Processor knows which harmonic of the Synthesizer frequency was used to generate the IF frequency being counted. The harmonic of the Synthesizer frequency is calculated from the 1st LO tuning DAC (digital-to-analog converter) code.since it indicates the 1st LO frequency to within approximately ±10 MHz.

Counting the 2nd LO frequency is much simpler. The controllable 16-20 MHz VCO in the 2nd LO assembly determines the frequency of the 2nd LO ; therefore, the 2nd LO frequency is calculated by directly counting the 16-20 MHz signal. The 2nd LO frequency is then calculated from this frequency.

Controlling the Oscillator Frequency—The frequency control loop is only closed between sweeps. After the completion of each sweep, the processor switches the span/div to zero and then counts the 1st LO and the 2nd LO frequencies. If they are not at the frequency required to generate the displayed center frequency, they are set to the correct frequency by repeating the process (i.e., the DACs are changed to tune the LO, the LO is counted, etc.).

In the single sweep mode, the oscillator frequencies are corrected after each single-sweep actuation, and before the sweep starts. In the manual sweep mode, or other non-recurring sweeps, the oscillators are corrected at periodic intervals.

Counting the IF—In addition to counting the frequency of the 1st and 2nd LO, the 10 MHz IF is counted when the Counter mode is actuated; thus, the incoming signal frequency can be calculated from the frequency conversion equation for the analyzer. The 1st LO is actually phase locked before the 2nd LO and IF are counted, in order to reduce FMing in the IF signal. This allows very accurate signal counting, even in wide spans.

HARMONIC MIXER 

The Harmonic Mixer combines a portion of the 2-6 GHZ 1st LO signal with harmonics of the 200-220 MHz reference signal from the Auxilliary Synthesizer to provide an output signal in the 10-80 MHz range. This signal is amplified and returned to the Auxiliary Synthesizer where it is counted to get an exact computation of the oscillator frequency. The Harmonic Mixer consists of a directional coupler, an input amplifier,the mixer, and an output amplifier, all on a hybrid alumina circuit. Figure 7-27 shows a functional block diagram of the Harmonic Mixer.

Input signal level, from the 1st LO to directional coupler A25A1, is a about +10 dBm. The coupling ratio is 10 dB, therefore, the coupler will deliver about 1 mW (0 dBm) to the RF input of the harmonic mixer. The through-port contributes about 0.5 dB of loss for the 2-6 GHz signal.

The 200-220 MHz reference signal,at a level of about 10 mW from the Auxilliary Synthesizer, is amplified to a level of about 100 mW (+20 dBm) by a differential amplifier Q1 and Q2. Resistor R27 couples the emitters together and the current is set by R13 and R14. Output is transformer coupled to the input of the mixer. Input signal level to the amplifier is −7 dBm minimun.

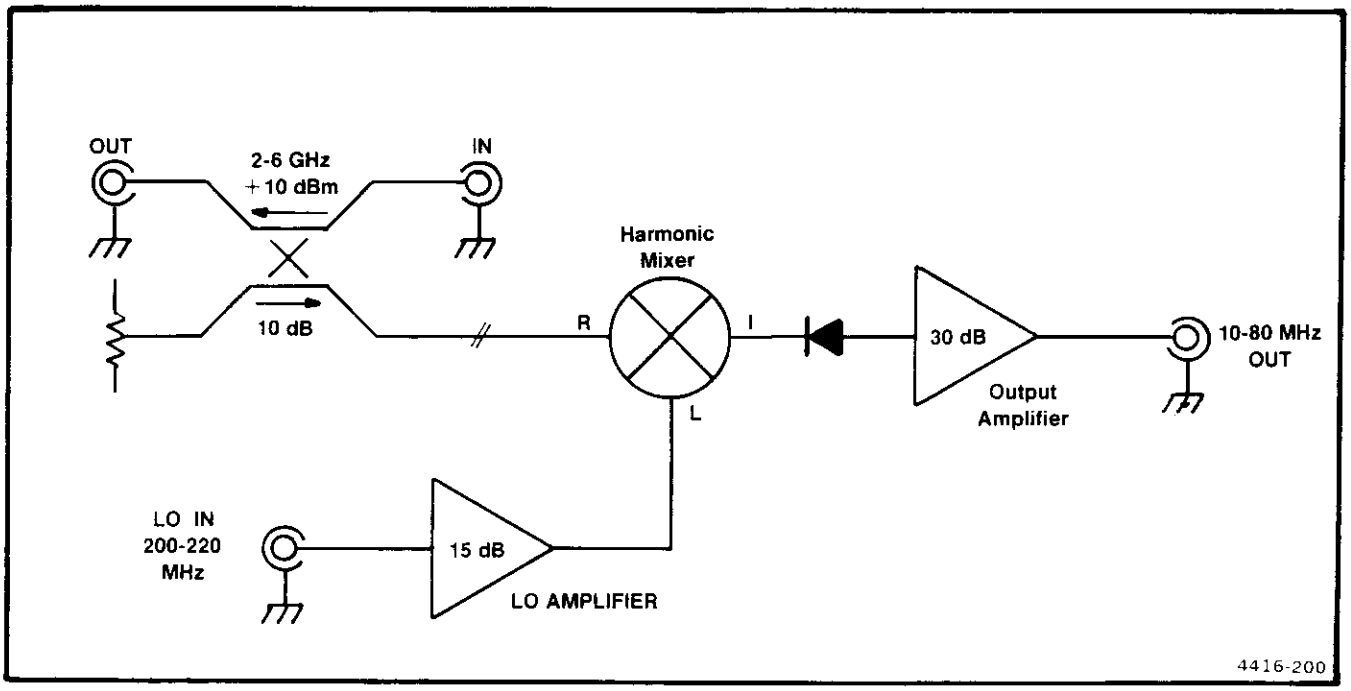


Figure 7-27. Simplified schematic of harmonic mixer.

Two additional directional couplers are used to couple the 2-6 GHz signal into the mixer circuit.A power splitter (R1, R2, R3) splits the signal into two paths . Each signal (approximately −6 dBm each) is then coupled through these couplers to the mixer. The through ports are terminated in 50 Ω. Thus the 2-6 GHz signal is coupled into the mixer differentially at a power level of about −16 dBm.

The 200-220 MHz reference signal is also coupled differentially into the mixer circuit, since the output of transformer T1 is applied across the two terminating resistors R4 and R5. The level of this signal is high enough to drive the snap-off diode into its operational region. Harmonics of this 200-220 MHz signal mix with the 2-6 GHz signal to generate numerous IF products which are detected by diodes CR2 and CR3 and fed to the output amplifier.

The output amplifier is a two stage common-emitter cascade amplifier with dc coupling between stages. The standing current through the second stage (Q4) is higher than in the first stage (Q3) to provide better power and IM performance. The amplifier is designed for a 10 to 80 MHz response. Signals above 80 MHz are rejected by a low-pass filter in the Auxiliary Synthesizer. Output level of signals in the 10-80 MHZ range is typically −20 dBm for input signal levels as described.

AUXILIARY SYNTHESIZER

The Auxiliary Synthesizer is part of the Direct Frequency Readout (DFR) system for the 494. This, along with a harmonic mixer, counter circuits, supporting filters and amplifiers, and appropriate firmware, make up the DFR or integrated microwave counter. The DFR provides the means for measuring and determining the frequency of all oscillators and the center of the IF, so the center screen frequency is always known. Since the IF signal can be counted, this allows direct frequency measurememt of any signal applied to the input port of the 494.

A functional block diagram of a simple or basic synthesizer is shown in Figure 7-28. The VCO frequency is divided by "N" in a programmable down-counter which outputs a pulse every Nth input pulse. This frequency along with a frequency reference is then fed to a phase/frequency detector. The difference between the two signals is filtered and fed back as a control voltage to the VCO to phaselock the oscillator to the reference. The VCO frequency is related to the reference by, $F_{ref} = NF_{ref}$. As N is changed the VCO frequency will change by F_{ref} for each step in N. This produces outputs separated by F_{ref} . To get closely spaced channels, in tuning the VCO, the reference frequency must be relatively low.

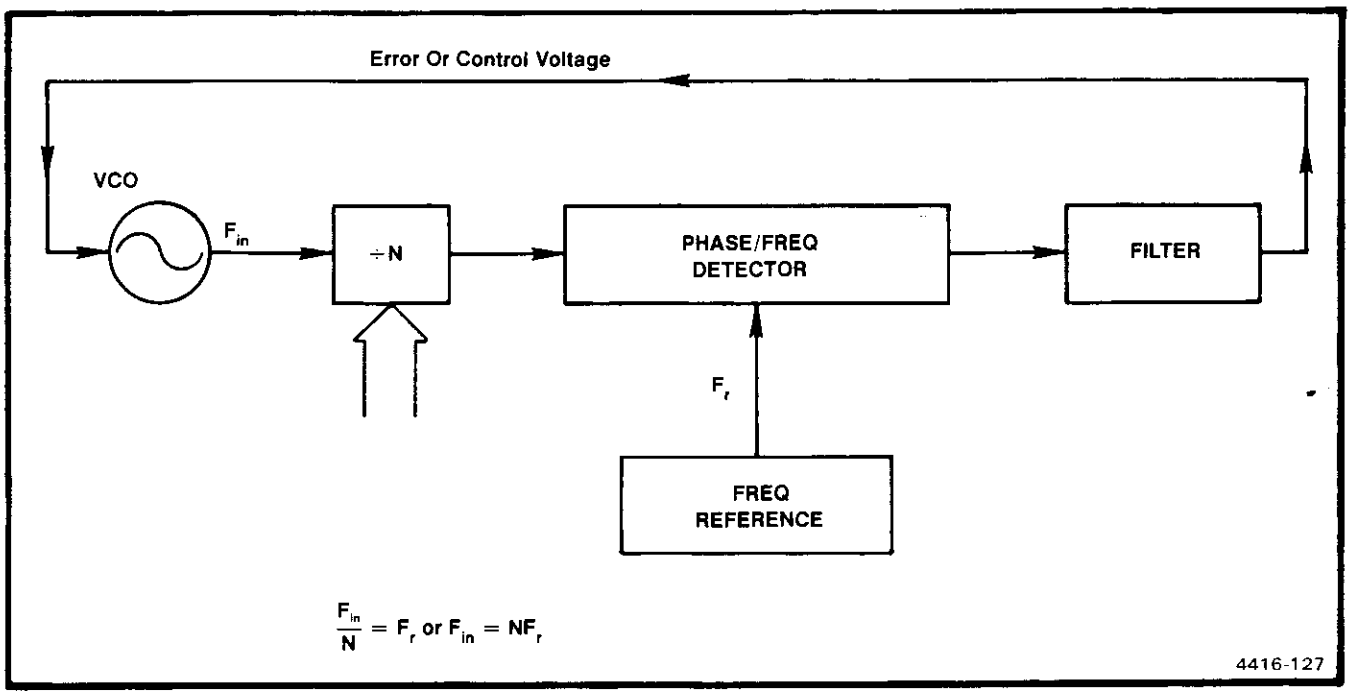


Figure 7-28. Block diagram of a basic synthesizer.

The synthesizer in the 494 uses a variable modulus prescaler to divide the frequency of the VCO down before is processed by the "÷N" counter, such as shown in Figure 7-29. The variable modulus prescaler is controlled by a modulus control input. When the line is high the prescaler is a divide by P+1 and when the line is low the division changes to P. A common type of prescaler is a divide by 10/11. A cycle of system operation starts with all programmable counters loaded and ready to count. The variable modulus prescaler initially divides by P+1.

Two programmable dividers are used with this system, both triggered by the output of the prescaler. One is a ÷N, with N being a relatively large number, the other is a "÷A", where A is a small number. One possible state includes A = 0.

The operation of this system is as follows: The lower case letters represent variables, the upper case letters represent the programmed values. At the beginning of the cycle, p=P+1, a=A, and n=N. Afer P+1 pulses from the VCO, one pulse is applied to the "a" and "n" counters and "a" and "n" decrease by 1 (a = A-1,n = N-1) This continues until a = 0 at which time the modulus control line changes state and p = P while n = N-A. The counting continues until n = 0. Both the "n" and "a" counters now return to the programmed condition. The total number of pulses applied from the VCO is:

$$N_{total} = (P+1)A + P(N-A) = A + PN$$

Both N and A are programmable so; $F_{vco} = (A + PN)F_{ref}$. This leads to a possible channel spacing of F_{ref}, obtained by changing A by 1.

A functional block diagram of the Auxiliary Synthesizer is shown adjacent to the schematic in the diagrams section. The VCO (Q2071) is configured in a Colpitts oscillator circuit with the inductance as a three turn air core coil with feedback provided by C2072 and C2071. Coarse tuning is accomplished with C1070, while the voltage control of the frequency comes from the varactor diode, CR2068. This diode provides a frequency shift of over 30 MHz from a voltage swing of +5 to +11 V, which is ample overlap for the 20 MHz tuning range.The output power of the oscillator is 0 dBm into 50 Ω. The oscillator is biased so it can be turned off and on rapidly.

The VCO is turned off by turning Q2076 on. In operation, the synthesizer is turned off during periods when information is presented on the crt. Synthesis and counting is done during retrace time to prevent possible interference on the display from any radiated energy from the synthesizer.

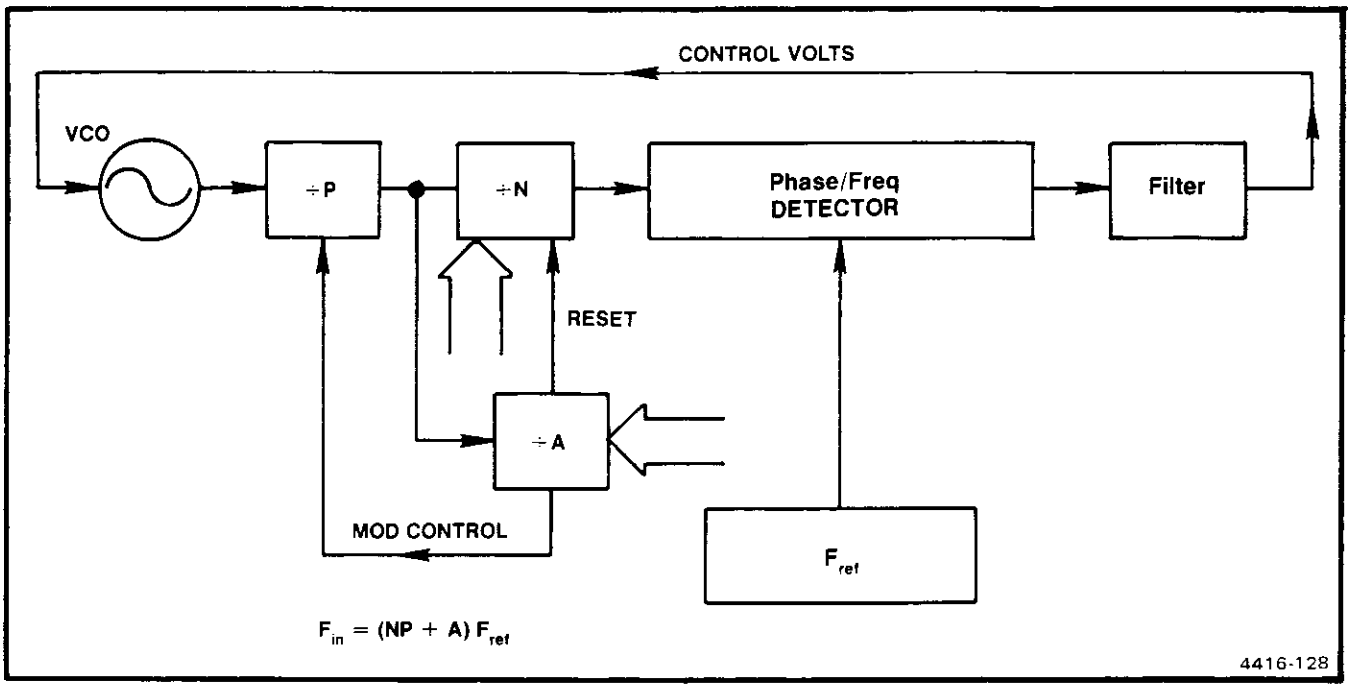


Figure 7-29. Basic block diagram of a ÷N synthesizer with a variable modulus prescaler.

The VCO output is split by a resistive power divider. One output drives transistor U2058, which provides +7 dBm of signal output to the Harmonic Mixer. This device is biased to a 20 mA collector current by transistor Q2055.

The other VCO output drives a low gain amplifier, Q2049, which is biased by transistor Q2051.Negative feedback, in the form of emitter degeneration and shunt current feedback, sets and stabilizes the gain to ensure stability with regards to spurious oscillations. The output of Q2049, to drive the variable modulus prescaler is 0 dBm. The variable modulus prescaler U3051, is a ÷32/33 IC that features an ECL input with a TTL or CMOS compatible output.

The major circuit of the synthesizer is U4041, a Motorola MC-145146. This IC is a large scale integration CMOS device intended for frequency synthesis applications with a variable modulus prescaler. U4041 contains three programmable counters; a ÷N, a modulus control counter ÷A, and a reference divider which divides an input from a crystal controlled source or other reference frequency down to a desired frequency. This CMOS device has a speed comparable to TTL. It also contains a phase-frequency detector which drives an external loop filter that uses an operational amplifier. U4041 will accept data for N,A, and R inputs from a 4-bit data bus while a 3-bit address bus selects the information to be loaded. Data contained on instrument bus lines DB4 to DB7 is loaded when the enable line goes high. Address information is contained on instrument bus lines DB0, DB1, and DB2. The appropriate 32 latches are also contained within this IC.

The output from the phase/frequency detector in U4041 is a chain of pulse signals at the reference frequency.The pulses contain both ac and dc components. The ac part of the signal causes reference sidebands to appear on the VCO output. These sidebands are suppressed by two active loop filters consisting of U2040A and U2040B. The outputs (0_{Ref} and 0_{Var}) from the detector,which are similar but with reversed polarity, are applied differentially to the input of U2040A. Slight differences in pulse width between the two outputs generate a dc voltage which is further filtered, to suppress frequencies above 20 kHz, by an active low-pass filter (U2040B) before it is applied to the varactor diode CR2068 in the 200-220 MHz VCO.

U2040A is an integrator with a series resistor added to the feedback capacitor. This controls the slope of the loop gain at gain crossover. To provide additional suppression of the reference sidebands, an RC active two pole filter, U2040B, is added. Cutoff frequency is about 20 kHz. The loop filter (U2040A) and the VCO provide the dominent poles that determine the system response. A damping factor near unity provides the stability. Additional filtering in the form of passive components, with a high frequency cutoff,are added between the output of U2038B and the varactor diode CR2068. CR1065 provides a clamp to prevent a control line voltage less than 5 V. Capacitor C1070 sets the low end of the control voltage to about 6 V. Range of the control voltage, over the 200-220 MHz VCO range, is about +6 to +11 V.

The off/on status of the VCO is controlled by U4074 which is activated by D3 from the data bus. The value is latched in U4074 and its output turns Q2076 off or on. The output also controls the sensitivity of divider U5015. During the period when the VCO is off and there is no input signal, the divider sensitivity is lowered so stray signals will not activate the divider. This is done by turning Q5027 on and pulling input pin 6 of U5015 low.

The 100 MHz signal from the 3rd converter is applied through a resistive power splitter to divider U2017 and to buffer amplifier Q1015. The 1 MHz output from the divider, U2017, is futher divided by 5 within the synthesizer IC, to become the 200 kHz reference frequency for the synthesizer. The amplifier Q1015 has negative feedback for gain stabilization. Its output signal is applied to the counter board.

The 10-80 MHz signal from the harmonic mixer is passed through a 7-pole low-pass filter with 80 MHz cutoff. The signal is then amplified by U4021 with a broad band gain of about 24 dB.

COUNTER BOARD

The Counter board circuits and function are: 1) The address decoder which receives and decodes the talk and listen commands for the microcomputer. 2) The service request circuits that sense an impending loss of 1st LO phase lock and sends a service request to the microcomputer. it then cancels the request when directed by the microcomputer. 3) The data buffers transmit data to and from the microcomputer. 4) The input amplifiers and multiplexer amplify input signals up to TTL levels and then select which of the input signals is to be counted. 5) The $\div 2^n$ counter divides the selected input signal by some power of 2 as determined by the microcomputer. 6) The 21-bit counter counts at a 100 MHz rate for a given number of cycles of the selected input signal.

Address Decoder

The addresses from the microcomputer are decoded by address decoder U2040. The counter circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U3024 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U3040, latch U3048B, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far. The UP and DOWN signals from the window comparator (located on the Error Amplifier board) drive NOR gate U3010C. Both signals are also sent to U3034, where their status can be read by the microcomputer. When one of these signals is high, it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U3010C produces a negative transistion that is inverted by U3046C. C2050 pulls the set input of U3048B high for approximately 10 μs. The Q output of U3048B then goes high, causing Q4052 to pull the SR (service request) line low.

The $\overline{Q}$ output of U3048B pulls the $G\overline{1}$ and $G\overline{2}$ inputs of multiplexer U3040 low, enabling both sides. This device allows Q4034 and U3048B to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which is to pull the POLL signal and AB7 high, then interogate each data bus line in succession to determine which address requested service; i.e., which data line is low. To do this, the Y1 output of U3040 is set high, which causes Q4034 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the Y2 line from U3040, clocks U3048B to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request because it cuts off Q4052 permits its output to move high. In addition, the complement output of U3048B moves high, which disables the inputs to U3040. This brings the service request circuitry back to its original state.

Data Buffers

The data buffers consist of U3024, U3034, U3030, and U2026. U3024 is the listen buffer. When address decoder U2040 is addressed by the microcomputer to listen,, it enables U3024, which passes on the buffered data to the other circuits in the Counter board. The function of each data bit is as follows.

D0—This line carries the serial data that selects which input signal is to be counted and what n numbers to use in the $\div 2^n$ counter. This data is loaded into shift register U1022. D0 also carries the data for the $\div$N counter in the Phase Lock Synthesizer circuits.

D1—The N LATCH signal for the 1st LO phase lock is sent on this line.

D2—Reserved for future applications.

D3—This line resets the buffer sequencer at the outset of a talk cycle for the counters.

D4—This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5—This signal clears all the counter stages in the counter-buffer circuits in preparation for a count sequence.

D6—This line latches the N data in U1022.

D7—This line is used as a clock to step data into U1022 and U3048A, and for the data sent in the 1st LO phase lock. R3012 and C2010 act as a delay to provide adequate setup time for the data prior to the clock signal arriving.

Buffers U3034, U3030, and U2026 are the talk buffers that send data to the microcomputer. U3018 and U2030A make up a step-enabler that enables the talk buffers one at a time when requested by the microcomputer.

Input Amplifiers and Multiplexer

Q1018 brings the −5 dBm, 16 MHz to 20 MHz signal from the 2nd LO up to TTL levels. U2010 divides the 16-20 MHz by 32 and 256 before it sends it to multiplexer U1018. U2056 amplifies the −50 dBm, 10 MHz IF. L2056 and C2056 act as a 10 MHz bandpass filter on the input of U2056. R3056 provides current to the open collector output of U2056. C3052 couples the 10 MHz signal into U4056. U4056 acts as a divide-by-128 counter. The signal then goes to U1018.

All other input signals are at TTL levels and are connected directly to U1018. The ouput of U3010A is connected to U1018 so that the clock can be counted for diagnostic purposes. U1018 selects one of its inputs according to the data in U1022.

÷2^n Counter

The output of U1018 goes into a series of dividers made up of U1050 and U2050A. Various outputs of these dividers are connected to mulitplexer U1046 to give a ÷2^n) counter where n = 1, 2, 4, 6, 8, 10, 11, or 12 (n is selected by the data stored in U1022). A strobe input to U1046 disables the multiplexer when pulled high.

21-Bit Counter

The 21-bit counter counts the 100 MHz reference frequency to give a measurement of the time required to complete a given number of cycles of the selected input signal. The counter itself consists of U1038, U2018, U1028, and U2034. U1038 is an ECL divider. Q1034 and Q1044 are ECL-to-TTL translators for the ÷2 and ÷4, respectively. The ÷4 goes to U2018 where it is counted with TTL dividers, and the divider chain continues through U2034. The output of each stage goes to an ouput buffer so the microcomputer can read the final number of counts. Therefore, measure the time period during which the counter was enabled. The counter is enabled by U2050B and U2046 for a time period equal to eight cycles of the output of the ÷2^n counter.

At the start of a count, the microcomputer selects the input signal to be counted and selects the n number for the ÷2^n counter. The $\overline{\text{COUNT}}$/RESET line is then pulled high to reset all of the counters. U2046A is preset with Q in the high state, which disables the 21-bit counter. The $\overline{\text{COUNT}}$/RESET line then goes high to start the measurement process. The output of U1046 goes to U2050B where it is further divided down. On the first rising edge at QA of U2050B, Q of U2046A goes low to start the 21-bit counter. On the eighth count of U2050B, U2046A steps back to its original state, which stops the 21-bit counter. At the same time, U2046B pulls the strobe to the ÷2^n counter high to stop any further counts in U2050B. The microcomputer can now read the VALID COUNT line to determine when the count process is completed, and then read the data that is stored in the 21-bit counter.

PHASE LOCK SYNTHESIZER ◈39◈ ◈40◈

The Phase Lock Synthesizer consists of: the Error Amplifier, the Synthesizer, Offset Mixer, Controlled Oscillator, and Strobe Driver. The following describes the circuits and their function.

Synthesizer ◈39◈

The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate the 25 MHz reference frequency for the Offset Mixer and the ÷N frequency (determined by the N number from the Processor) for the phase/frequency detector in the Offset Mixer. The ÷N number is within the 32 to 94 kHz range.

The Synthesizer can be divided into three functional blocks: the 100 MHz divider, the 50 MHz divider, and the ÷N counter.

The 100 MHz divider consists of flip-flop U3030 and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The 50 MHz signal from the Q output is applied through buffer amplifier Q3041 to P500; it is not used in the 494. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

The 50 MHz divider consists of the flip-flop U1040B. The 50 MHz from the collector of Q3040 is applied to the clock input of U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the ÷N counter.

The ÷N counter consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer via the Counter board.The output of the ÷N counter is a frequency within the range of 32 to 94 kHz which is applied to the phase/frequency detector in the Offset Mixer. When power is first applied, and before phase lock is selected, this counter typically outputs a frequency of approximately 6 kHz.

When phase lock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The numbers that come from the microcomputer, range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. The TC output of U1030 then moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μs to 31 μs which is equivalent to 94 to 32 kHz. This signal is sent to the phase/frequency detector in the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

ERROR AMPLIFIER, CONTROLLED OSCILLATOR, OFFSET MIXER, AND STROBE DRIVER ◈40◈

Error Amplifier

The Error Amplifier: 1) Integrates the error signals from the Offset Mixer and produces a correction voltage to pull the VCO to a frequency that is synchronous with the ÷N signal. 2) Generates a STROBE ENABLE to enable the strobe generator in the Strobe Driver circuit. 3) Produces an UP or DOWN signal to alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phase lock. 4) Generates an F ERROR signal, from the outer loop ERROR 1 signal, to be used by the Counter board for diagnostics. 5) Provides the F(s) amplifier for the outer loop.

The digital control circuits consist of shift register U2025 and quad switch U2037. Data from the microcomputer is fed serially, via the Counter board circuits, into the shift register, then transferred to the output lines by the CONTROL LATCH signal. Table 7-21 lists the purpose of the output lines.

Differential amplifier,U3075 compares the FsB and FsA outputs from the phase/frequency detector on the Offset Mixer board and furnishes the oscillator tune voltage for the VCO. Refer to the Offset Mixer description that follows, for a more detailed description of this circuit.

Table 7-21
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled (Q5 low)	Wide window (Q5 low)
Q2	Lock (connected FM coil)	Unlock (disconnected FM coil)
Q3	Wide loop gain response	Narrow loop gain response
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window (with Q1 low)

The loop amplifier circuit consists of amplifier U2048 and surrounding components. The ERROR 1 signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR 1) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR 1 signal varies from zero to about 500 kHz, and is up to four volts peak-to-peak in amplitude.

When phase lock is not required, data into U2025 sets output Q2 and Q4 low and Q3 high. This opens the connection between pins 11 and 10 of U2037 and the connection between pins 2 and 3. STROBE ENABLE line to the Strobe Driver goes high and disables the strobe pulse. The FM coil of the oscillator is opened by U2037 which opens the outer loop.

To establish phase lock,the microprocessor sets the 1st LO near the desired lock point and loads the proper N number into the synthesizer. The 5 MHz strobe is then turned on (Q4 and Q2 output of U2025 set high) and the microprocessor tunes the 1st LO up or down 750 kHz either side of the desired lock point at a 10 Hz rate. When the oscillator frequency crosses the desired lock point, the ERROR 1 frequency is reduced to a dc voltage which results in U2048 pulling the 1st LO in the direction required to maintain a constant frequency. When the microporcessor measures the 1st LO frequency and finds it held constant, at the desired frequency, it then sets Q3 output of U2025 low to reduce the bandwidth of the phase lock loop.

Window comparator, consisting of U1015 and the associated components, is used to sense when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR 1 signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and Q5 to be low, closing the contacts that connect the output of U2048 to the input of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the loop amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its design limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator that senses a deviation of ± 15 mV. For example,if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Counter board, which in turn alerts the microcomputer so it begins adjusting the TUNE voltage from the Center Frequency Control circuits to reduce U2048 output to zero. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Normally, the input signal to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048. This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phase lock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phase lock is cancelled.

The ERROR signal filter circuit, consists of an active low-pass filter U2065 and Schmitt trigger U1035. This circuit filters and squares the incoming ERROR 1 signal for application to the Counter board. The ERROR 1 signal is applied through C2067 to an RC, 500 kHz, low-pass filter and amplifier U2065. After filtering, the signal is applied through Error Count Breakpoint adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to circuits on the Counter board, where it is used by the microcomputer for determining the relationship between 1st LO frequency and the strobe line.

Controlled Oscillator (VCO)

The Controlled Oscillator (VCO) is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency. Refer to the block diagram adjacent to Diagram 40 for a functional description of this part.

The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled ÷N signal and the Offset Mixer difference frequency, is applied to the VCO on the Controlled Oscillator board to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phase lock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the ÷N signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The VCO consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the band-pass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. The output signal from the resonator is applied to the input of a differential amplifier which drives the output amplifier and the band-pass filter. The output from the output amplifier is fed to the Offset Mixer and the Strobe Driver. The band-pass filter strips the signal of any spurii either side of center frequency and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the band-pass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within the frequency range of 25.032 to 25.094 MHz, which is controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, to the band-pass filter.

The band-pass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center the frequency of the filter.

The isolation amplifier, Q1028, is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier, consisting of transistors Q2025 and Q2026, is connected as a differential amplifier with Q2026 driving one side of the Offset Mixer and Q2025 driving the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Offset Mixer

The Offset Mixer consists of a ring diode mixer circuit, a differential amplifier, and a phase/frequency detector. For explanatory purposes, assume that the Controlled Oscillator (VCO) frequency is at 25.06 MHz and the ÷N signal is 50 kHz. The 25.06 MHz signal from the VCO enters the board at pin N of the Offset Mixer assembly. It is applied to the base of transistor Q2021 which drives transformer T2010. The output of T2010 is connected across the ring diode mixer. The 25 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. The two fundamental frequencies and the sum are blocked by a π filter, and the 60 kHz difference is coupled across T2030 to a differential pair Q1020/Q1030, then amplified to TTL levels by amplifier Q1040 and applied to the clock input of flip-flop U1050B (part of the phase/frequency detector).

The phase/frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. This results in a series of pulses of equal amplitude and width from each of the flip-flops which, when applied to the Error Amplifier, would not shift the frequency of the VCO.

It is assumed, however, that the ÷N signal is 50 kHz and the difference frequency from the collector of Q1040 is 60 kHz. Thus, the output of Q1040 is leading the ÷N signal. U1050B will "set" first, placing a high at the inverting input of U3075. This pulls the output of U3075 low until U1050A sets. A short time later U2050B resets both flip-flops and U3075 will switch back, until the next correction cycle. This process continues until the two signals, applied to the Phase/Frequency Detector, are edge coincident.

The correction voltage, in this example, from U3075, is applied to the frequency determining components of the VCO and its frequency shifts downward. The frequency of the oscillator will continue to decrease until the output of U3075 is stable.

The Error Amplifier, is described here because it is an integral part of the inner loop. The stage consists of differential amplifier, U3075, with its two inputs being driven by the output of U1050A and U1050B. As the signals driving the amplifier continue toward one direction, the output of U3075 continues to drive the oscillator down in frequency. VR2065, CR3069, R2067, and C2072 clamp the output of U3075 to prevent forward biasing the varactor diode and stopping the oscillator.

Strobe Driver Circuit

The Strobe Driver circuit consists of counter U1022, bandpass filter FL2064, source follower Q2091, and AND gates U1091A and U1091B.

The VCO output is applied to the clock input of a ÷5 counter U1022. The STROBE ENABLE line from the Error Amplifier permits the counter to operate when the line is low and is the means by which the microcomputer can turn the strobe pulses on or off.The output of the counter is coupled through an impedance matching network consisting of C2030, L1031, C2033, and C1032, to the input of bandpass filter FL2064. The impedance matching circuit raises the line impedance to about 8200 ohms. The output of the filter drives another impedance matching network for the gate input of Q2091. The output of Q2091 drives two buffer amplifiers U1091A and U1091B. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 and C2105 are selected to provide maximum signal amplitude at TP2087.

DIGITAL CONTROL SECTION

The Digital Control section provides the operator/494 and digital controller/494 interfaces. It translates changes in front-panel controls and instructions received, via the accessories interface or GPIB interface (494P only), into codes that control the instrument via the instrument bus.

The Digital Control section simplifies operating and programming the 494 and 494P. Unless overridden by the operator, the microcomputer automatically selects secondary parameters. Some examples are: when the operator selects span, the microcomputer chooses an appropriate bandwidth; when the operator changes the reference level, the microcomputer trades off input attenuation and IF gain.

The microcomputer can also perform many operations automatically, such as; automatic peaking, centering signals in the span, and directing the user through a calibration procedure.

The digital control operating program is defined by the meaning of the controls and commands given in the operating and programming manuals and is not further defined here. The following description focuses on the hardware for the following major circuits that comprise the digital control section:

1. Microcomputer, including Processor and Memory boards.
2. Addressable registers on the instrument bus.
3. Front panel.
4. Accessories interface.
5. GPIB interface (494P only).

MICROCOMPUTER

The microcomputer consists of a Motorola 6802 microprocessor, a 6840 timer IC, a 6821 PIA IC,a 9914 GPIA interface, 48K bytes of EPROM, and 14K bytes of RAM. An additional 96K bytes of EPROM is bank-switched between addresses 4000 and 8000 (hex). Switches are provided to modify the instrument configuration for performing self diagnostics. Refer to the appropriate Motorola or Texas Instruments data sheet for descriptions of the microprocessor and the three peripheral devices.

Storage of the instrument front panel control settings and displays is provided by 6K bytes of battery-powered RAM. This is CMOS RAM in 2K x 8 chips, powered by a 5 V line when the instrument is operating and by a 3 V lithium battery when the instrument is turned off. An additional 8K of RAM is provided for use by the instrument operating system.

The microprocessor (U1034) communicates with the memory and I/O ports via the microprocessor bus and with the rest of the instrument via the instrument bus. The microcomputer bus consists of 8 data lines (D0-D8), 16 address lines (A0-A15), a VMA line, the R/W (read/write) line, the $\phi 2$ clock line, and the RESET line.

The microprocessor communicates with the instrument bus through a 6821 PIA IC (U2010). The instrument bus consists of 8 data lines (DB0-DB7 Table 7-22), 8 address lines (AB0-AB7), a POLL line, a DATA VALID line and a SER REQ line.

Additional control lines connect different portions of the processor system: a GPIB SRQ line, a SWP GATE line, a PWR FAIL line, a CRT CLK line, an I/O (3XXX) line, and the INTL CONT line.

Interrupts are handled by the microprocessor in the following manner. Interrupts can be generated by hardware on the instrument bus, the GPIA interface IC, or the 6840 timer IC. The 6802 will first determine which of the three sources initiated the interrupt. If the interrupt is on the instrument bus, the 6802 initiates a poll routine to determine the particular piece of hardware, on the instrument bus, that generated the interrupt.

The instrument bus poll sequence is as follows: When an interrupt is received, from the instrument bus, the microcomputer puts an FF (hex) on the instrument address lines. This sets the poll circuits to reply. The microcomputer then raises the POLL line and asserts DATA VALID. At this point, the circuit that generated the interrupt asserts its respective bit on the instrument data bus. The microcomputer reads the data bus and remembers the bit. The poll line is lowered, then address 7F is put on the address bus. The data valid line is then raised. This sets up the poll circuits to receive the poll bit in reply. The microcomputer now writes the poll bit back on the data bus and the circuit that initiated the interrupt, resets and removes the interrupt signal. The microcomputer then services the interrupt.

TABLE 7-22
LIST OF POLL BITS

Bit 7	Not used
Bit 6	Reference Lock module
Bit 5	Not Used
Bit 4	End Of Sweep
Bit 3	CENTER FREQUENCY knob
Bit 2	Phase Lock
Bit 1	Not used
Bit 0	Front Panel

Figure 7-30 (System Memory Map) depicts the entire address range of the processor, including the bank-switched EPROM's between 4000 and 8000. The diagnostic LED's are at addresses 0800 to 3800.

Figure 7-31 (I/O Address Map) depicts the address range between 3800 and 4000. Data is transferred between the microprocessor and various external systems (instrument bus, GPIB bus, switches, etc.) within this range. Most of the addresses are unused; this is shown by the stippled areas of the address range.

Figure 7-32 (PIA & Timer Address Map) show details of the PIA and Timer address structure.

PROCESSOR BOARD

The 6802 processor (U1034) has its data lines buffered by U1026, a bi-directional bus transceiver IC.The processor address lines are buffered by U2032 and U2028. In addition, gates on U2024 are used to buffer the $\overline{R/W}$, the VMA, the CLOCK ENABLE, and the RESET lines.

The 6821 PIA IC (U2010) is used by the processor to interface with the instrument bus. This IC is buffered from the instrument bus by, U2012 for the address lines, and bi-directional buffer U2018, for the PIA data lines. Other gates within U2024, buffer the POLL line and the DATA VALID line. The direction of data through U2018 is controlled by the most significant bit of the instrument address bus. (As a result, all instrument bus addresses above 7F are read addresses and all addresses including 7F and below are write addresses.)

Y1036, Q1036, and Q2038 make up a discrete device clock circuit that oscillates at a frequency of 3.4133 MHz. Q1036 and Y1036 form a Colpitts crystal oscillator which is buffered and conditioned by Q2038 to give a TTL compatible clock signal. This signal is further buffered by a gate on U2024 before is is applied to the E XTAL input of the microprocessor. This frequency is divided by four, within the microprocessor, and called the $\phi 2$ (enable) clock. It is used by other devices on the microprocessor bus. The 3.4133 MHz clock is called the CRT CLK and is used by the Crt Readout board and the GPIA interface IC on the GPIB board.

U1016 is a programmable timer and counter that is used by the micro- processor U1034 as a timer to generate variable time delays. In this mode, the processor programs a given time interval into the timer and enables it. When the given time interval expires, the timer generates an interrupt and thus notifies the microprocessor. The clock signal for the timer is the $\phi 2$ clock line.

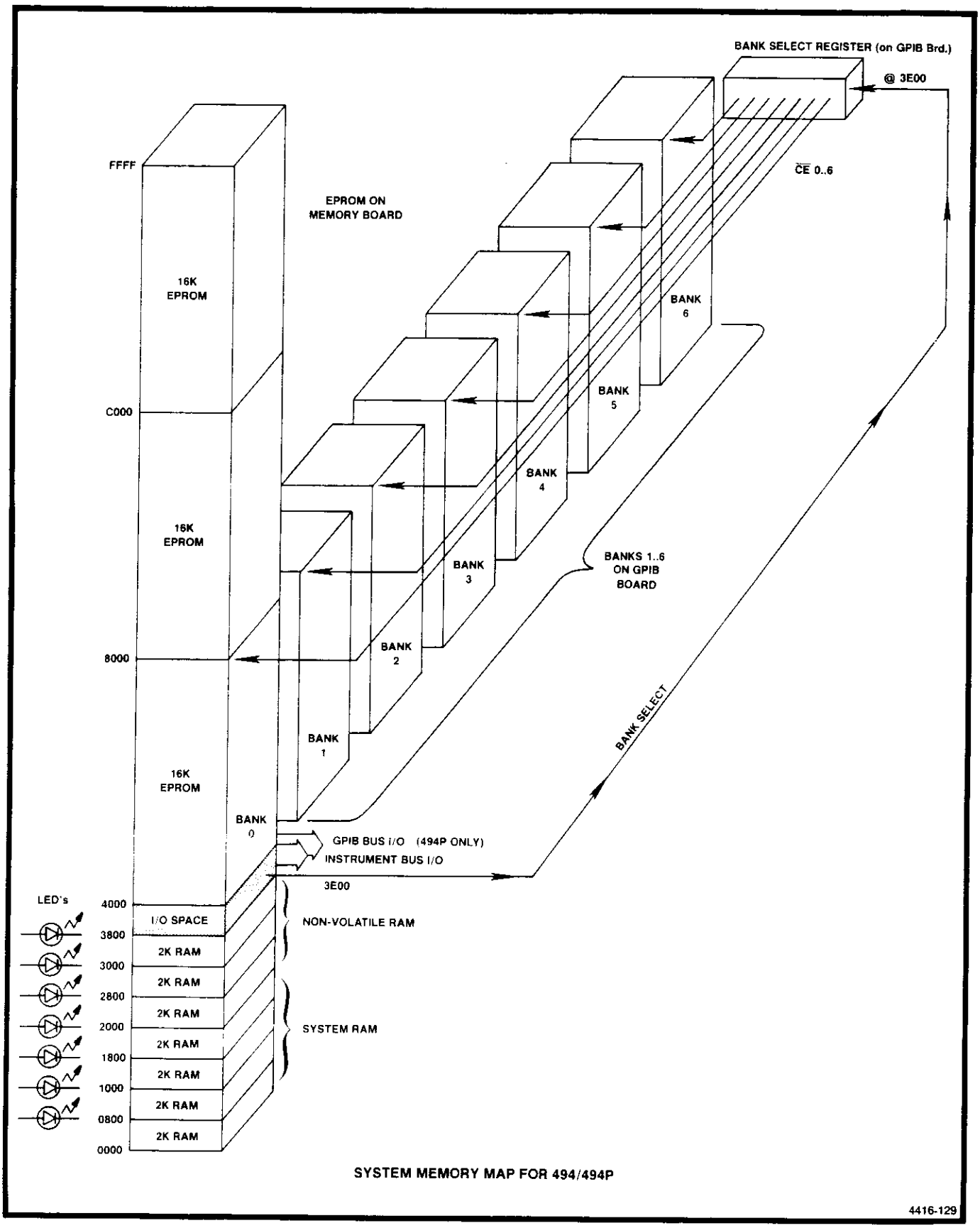


Figure 7-30. System memory map for 494/494P.

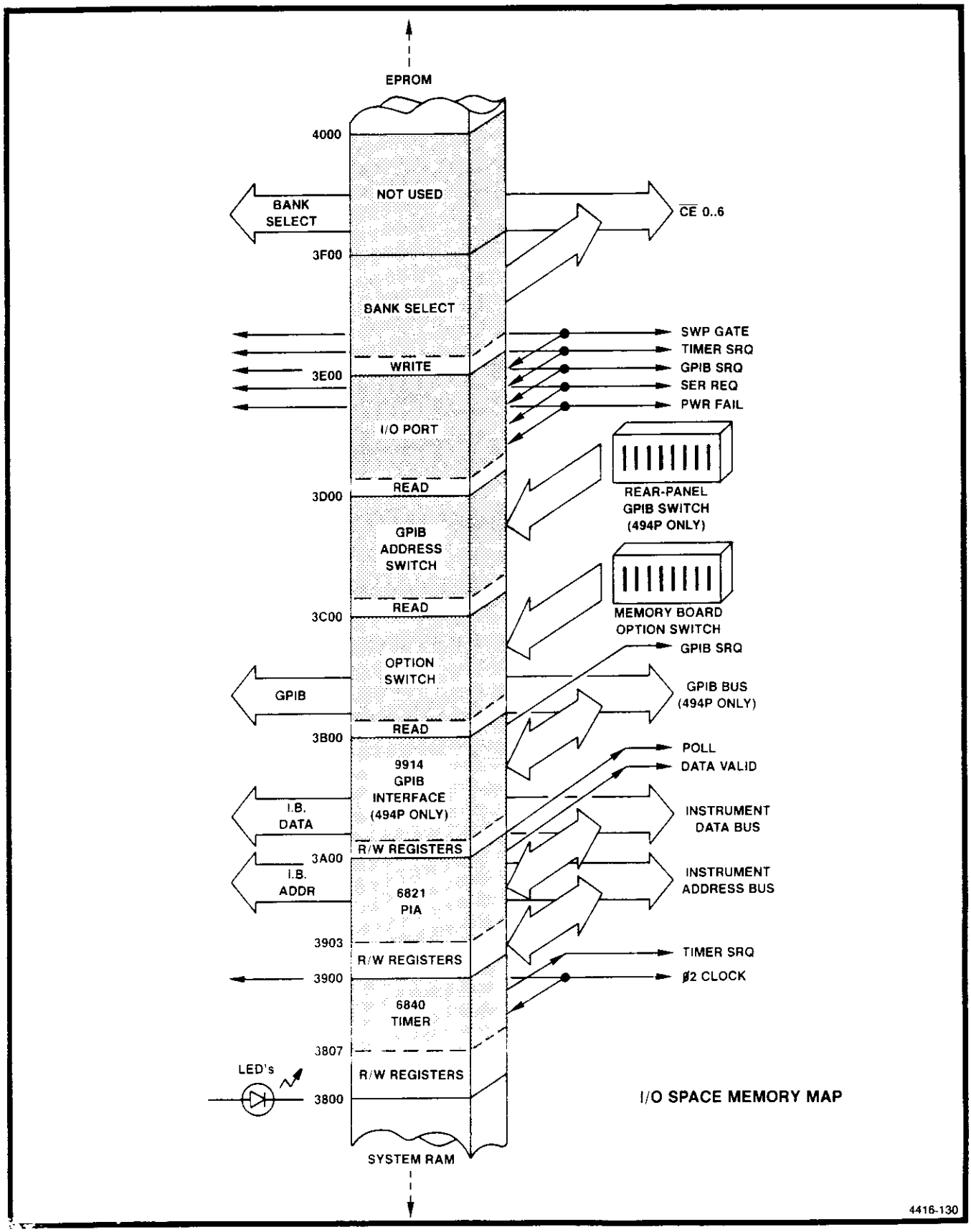


Figure 7-31. I/O space memory map.

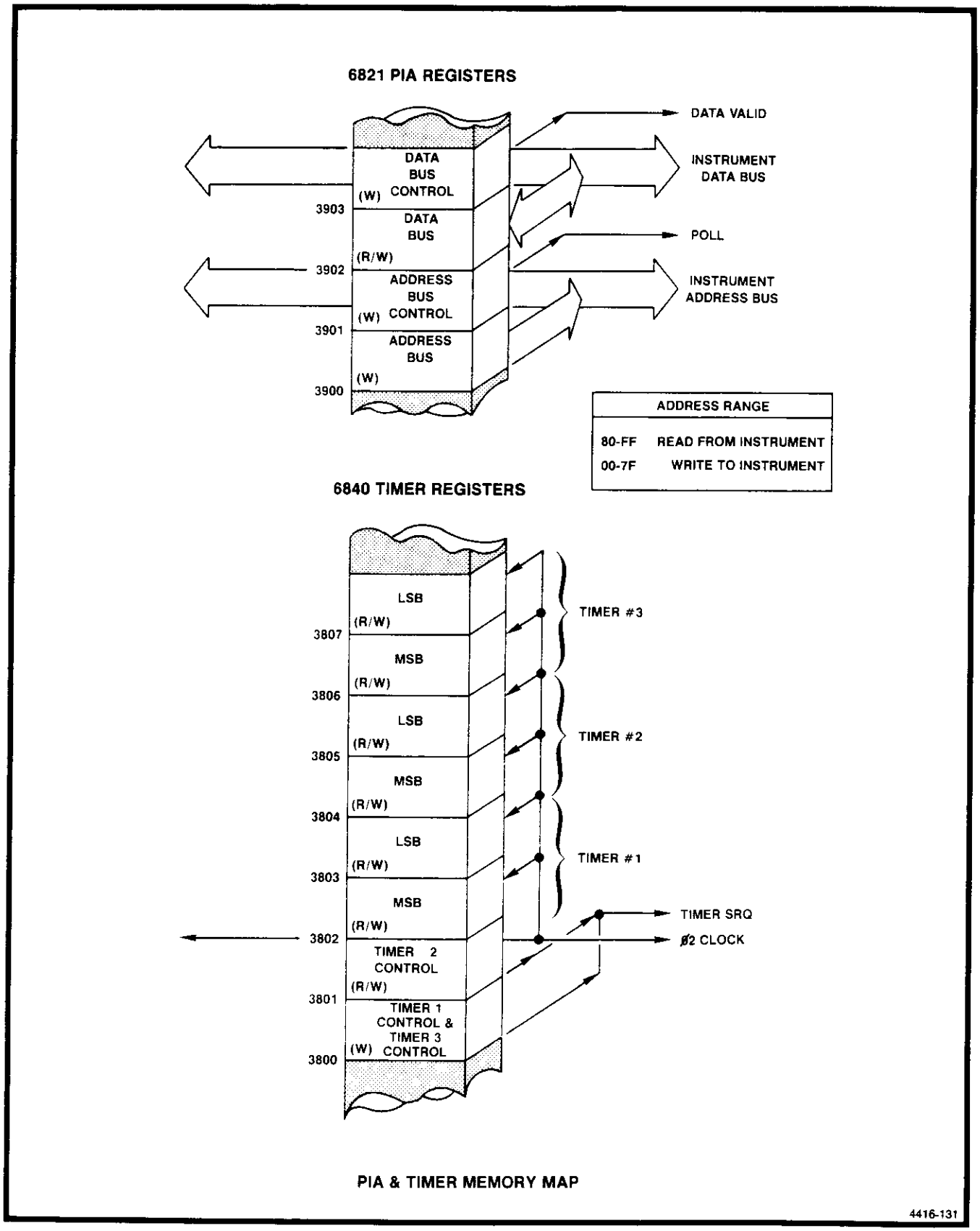


Figure 7-32. PIA and timer memory map.

U1020 is an address decoder that is activated by a signal derived from the Memory board. This signal is asserted when addresses from 3000 to 3FFF are asserted.The decoder further sorts addresses in this range and when address 38XX is asserted, the timer module is activated. When address 39XX is asserted, the PIA is activated. When address 3DXX is asserted, the I/O port (U1014) is activated.

U1014 is a tri-state buffer that is used by the microprocessor to monitor three interrupt lines and the sweep gate.

A circuit on the Z-Axis board monitors the power input ac line. If a power loss is detected,the PWR FAIL line goes low which tells the processor that power is about to fail. The PWR FAIL line is connected to the NMI (non-maskable interrupt) input on the processor and when the line goes low, the processor gets a non-maskable interrupt and starts its power-fail routine.

The PWR FAIL line is also applied, through a gate, within U2020 and Q2028, to the Reset input of U1034. When the PWR FAIL goes low, Q2028 is turned on and C1022 begins to discharge through R2022. If the line stays low for a period of time, the RESET line will also go low and the microprocessor resets itself if the power has been interrupted long enough to seriously disturb the logic power supplies. As part of its power down routine, the processor keeps checking the PWR FAIL line through U1014. If the PWR FAIL line returns to its high state, within the prescribed time, the processor will do a power-up initialization to ensure that the instrument operation will not be affected by a possibly low +5 V line to the various control latches.

MEMORY BOARD

The Memory board contains all the memory within the address range of 6802 processor. On this board are 48K bytes of ROM contained in three 16K byte EPROMs. These are Intel type 27128 EPROMS which can be programmed and then erased by exposure to ultraviolet light (see an Intel 27128 data sheet for a description of these EPROMs). There are also seven 2K byte CMOS RAMs, that comprise the read/write memory. To aid in self-diagnostics and instrument configuration, a set of LEDs and switches are provided.

U2044 (at 2000), U2037 (at 2800), and U2032 (at 3000) form the non-volatile 6K byte RAM system. Current requirements for each RAM is less than 1 μA these RAM's hold data as long as the V_{dd} voltage is above 2 V, referred to as the data retention mode.

The "D" flip-flop, U2049, is used by the processor to power-up and enable all the non-volatile RAMs. On initial turn-on, U2049 is reset by the $\overline{\text{RESET}}$ line. This causes the non-volatile RAM to remain in its data retention mode. After the processor has finished its initialization power-up sequence, it writes to the instrument address bus (73) to set U2049's output high. This allows C1045 to charge to +5 V and Q1042 and Q1043 are turned on. Q1042 turns on first and connects the V_{dd} input for the RAM to +5 V through Q1041. Q1043 then turns on and pulls $\overline{\text{CE2}}$ input low to take the RAM out of the data retention mode. If for some reason the processor crashes on power up, non-volatile RAM is protected from alteration since U2049 output will remain low.

On power-down the processor, after it completes tasks required for power-down (storing power-down settings in non-volatile RAMs and switching the RF attenuator to 60 dB attenuation), will set the output of U2049 low. This takes about 10 ms after $\overline{\text{POWER FAIL}}$ goes low. C1045 discharges and turns Q1043 and Q1042 off, which switches the V_{dd} input for the RAMs to the battery voltage backup supply on the GPIB board. At the same time the RAM's are switched to the data retention mode, since $\overline{\text{CE2}}$ is connected to V_{dd} through R1039 . About 60 ms after $\overline{\text{POWER FAIL}}$ goes low, the $\overline{\text{RESET}}$ line goes low and U2049 is reset to ensure that the RAM has been switched to the data retention mode, before power fails.

U2015 (at 4000), U1021 (at 8000), and U1014 (at C000) are the 27128 EPROMs. U2015 is wired to form bank 0 of the bank-switched ROM system.

U1036, U1046, and U1041 are address decoders. U1036 decodes the higher order addresses: 0000, 4000, 8000, and C000. U1046 decodes addresses for the RAMs at 0000, 0800, 1000, 1800, 2000, 2800, and 3000. U1041 is an address decoder for the I/O space. Address 3800 is used to access the Options switch.

U1036, S1038, and pull-up resistors in R1038, comprise the Options switch. Switches within S1038 can be set to configure different instruments, inform the processor of revised hardware, or initiate self diagnostics.

Light emitting diodes DS1043, DS1044, DS1045, DS1046, DS1047, DS1048, and DS1049, connected in the output lines of decoder U1046, are diagnostic LEDs used to indicate the results of the processor self-diagnostics.

GENERAL PURPOSE INTERFACE

The GPIB board contains ROM for the basic instrument functions as well as for the GPIB interface plus the GPIA to connect the microprocessor to the GPIB. The board also contains bank-switch circuitry for accessing additional ROM on this board and on the Memory board, plus a voltage back-up circuit for non-volatile RAM's on the Memory board.

Since the 6802 microprocessor is only capable of directly addressing 65,536 bytes of address space, 96K bytes of ROM on this board plus 16K on the Memory board, are addressed by a process called bank switching.

32K bytes of ROM (8000 to FFFF) on the Memory board are directly addressed by the processor. The remaining 112K bytes, stacked in banks 16K bytes wide and 7 deep, are accessed by means of bank switching. The bank number, from 0 to 6, is written by the processor to register U1033 at address 3E00. The number in the register is decoded by U1032 and its output turns the appropriate EPROM on. The processor can now access that EPROM in the usual manner at addresses 4000 to 7FFF. If the processor wishes to access another bank, it must first put a new number in the bank switch register U1033.

U1012, U1018, U1022, U1024, U2013, U2018, and U2022 comprise the bank-switched ROMs and consist of 16K byte EPROMs (Intel 27128's). These, plus U2015 on the Memory board, comprise the seven level bank as depicted in Table 7-23.

TABLE 7-23
LEVELS OF MEMORY BANK

Level 0	U2015 Memory board
Level 1	U1012 GPIB board
Level 2	U1018 GPIB board
Level 3	U1022 GPIB board
Level 4	U1024 GPIB board
Level 5	U2013 GPIB board
Level 6	U2018 GPIB board
Level 7	U2022 GPIB board

U1035 is an address decoder which provides addresses in the I/O space. It is driven from a decoder on the Memory board. Address 3E00 will access the bank switch register, address 3C00 the GPIB switches, and address 3A00 the GPIB interface IC U2036.

Tristate buffer U2027 is used to read the rear panel GPIB switches. Each input line is decoupled by a resistor capacitor combination to minimize noise and unwanted pulses. R2030 contains pull-up resistors for the lines.This buffer is accessed at address 3C00.

U2036 translates microprocessor commands, on the microcomputer bus, into appropriate codes and protocol for the GPIB bus. It also decodes data from the GPIB for the microcomputer bus. Interrupts are generated by pulling down on the GPIB SRQ line. The CRT CLK line provides the clock reference. This IC is accessed at address 3A00.

The voltage backup supply for the non-volatile RAM, consists of a small, high-energy, 3 V lithium battery (BT1022). During normal operation, when +5 V for the non-volatile RAM is supplied from the power supply, via Q1041 on the Memory board, CR1025 is reverse biased so the battery is protected from reverse charge. When a power failure occurs,the 5 V supply to the non-volatile RAM's on the Memory board deteriorates. CR1025 is then forward biased so power is provided from the battery for power-off data retention in the RAM's.

ACCESSORIES INTERFACE BOARD

The Accessories Interface board provides access to the instrument bus and input and output for two analog signals. This access, to the instrument bus, can be used for diagnostics or by other accessories.

The two analog signals are; an input MARKER/VIDEO, through a coaxial connector, an output EXT PRESEL and a EXT PRESEL RETURN (a differential signal on the ACCESSORIES connector). To display an external signal that is applied to the MARKER/VIDEO input, pull the EXT VIDEO SELECT line (pin 1 of the ACCESSORIES connecto low. The EXT PRESEL output will drive an external preselector. It is valid only in preselector bands (1.7 GHz to 21 GHz). This signal tracks the instantaneous frequency at a nominal 2.1 GHz/V with zero output corresponding to 2.072 GHz.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

Two lines, INT CONT and DATA BUS ENABLE define the 494/external device interface. INTL CONT is asserted low by an external controller to disable the internal microcomputer's instrument bus buffers. This sets the address buffer U2033 and control-lines buffer U2015, to drive the

address lines, DATA VALID and POLL lines, and listen to SER REQ. It also sets U2038 to indicate the direction of data through the data lines buffer U2025, depending on the sense of the MSB of address AB7. When INTL CONT line goes low, U2038 is set to drive the buffer in a manner similar to the Processor board data buffer—a write to the internal bus if AB7 is low and a read if AB7 is high. When INTL CONT is high, the buffer is enabled to write to the external bus when AB7 is low and read when AB7 is high.

The DATA BUS ENABLE line is asserted low by an external device to enable the data buffer. As long as this line is unasserted, the data buffer is set to its high impedance state and the data direction input has no effect on its output.

FRONT PANEL

The Front Panel board is an interface between the user and the instrument. It translates an operator action, of a front panel control, into data for the microcomputer to read and implement. It outputs data showing current operating modes to the user, via LED's and Crt readout.

NOTE

In this description, the front panel CPU (8741) or slave, is referred to as CPU. The instrument processor (6802) is the master processor or master microcomputer.

Output of data is provided by five shift registers that drive LED's (light emitting diodes) to illuminate various front panel push buttons and indicators to show the instrument operating mode. Operator input information,via push buttons or rotary switches, is read by the CPU. The front panel CPU then outputs the data to the master processor for action. The front panel CPU scans all push buttons and rotary selectors, on the keyboard matrix, plus the coder for the FREQUENCY knob, looking for changes in the keyboard codes or frequency coder. It then translates these changes into an appropriate code for the master processor so it can take appropriate action. The following is a description of the hardware and a brief description of the software used by the front panel CPU.

Potentiometers

The following controls or adjustments generate analog signals that are used by other functions of the instrument. These controls are non-programmable.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be either peak detected above or averaged below a displayed cursor line that tracks this control.

MANUAL SCAN sweeps the spectrum or display in manual sweep mode.

POSITION centers the horizontal and vertical deflection on the crt.

LOG/AMPL CAL varies the video signal level prior to the Video Processor board and adjusts 10 MHz IF gain to calibrate the log display.

PEAKING controls the front-end response of the analyzer by fine tuning the internal preselector or by varying the bias on an external mixer.

Output Mode Shift Registers and LED's

As previously described the mode of operation is illuminated by LED's that are mounted behind a pushbutton or below some front-panel nomenclature. There are 35 of these LED's. Some 49X versions may not use all indicators; for example,the non-programmable versions do not have a RESET TO LOCAL button.

The LED's are driven by shift registers (U5045, U6081, U6028, U6045, and U1049) that reside at address 74 on the instrument bus. The shift registers that drive the LEDs are reloaded each time a LED changes state. The master processor changes the appropriate bit in the LED code then reloads all registers. The shift register U6081 that drives the GRAT ILLUM, LED, also controls the voltage regulator U6090, which provides power for the graticule lights DS1011 and DS1013.

Processor

The CPU (Intel 8741) is a self-contained 8-bit processor with on-chip EPROM and RAM. (Refer to Intel UPI Users manual for a complete description of the 8741)

The IC has a self contained clock that uses Y3030 (a 6 MHz crystal) as the resonator, and a timer that functions either as a programmable timer or counter. The CPU has two input/output ports. Port P10-P17 is input only and P20-P27 in an input/output port. Each port is 8-bits wide. In addition, the CPU has an 8-bit data port (D0-D7) called the output buffer, which talks to the master processor.In this application all data is output only with U4030 being a buffer

between the CPU and the instrument bus.Information that the CPU wishes to relay to the master processor, is loaded into a latch connected to the output buffer U4030. The master processor accesses the CPU by pulling address F4, out of decoder U6024, low to activate the output buffer and enable U4030 so data is passed onto the instrument bus.

The CPU is reset by the master processor. When DB3 is selected for more than 10 ms (same as writing 08 at address 74) C1016 charges and U1024A output resets the CPU.

Scanning the Keyboard

The front panel keyboard contains 74 keys arranged in a matrix of 4 rows of 8 columns and 6 rows of 7 columns (see Figure 7-33). The RESOLUTION BANDWIDTH, SPAN/DIV, TIME/DIV, MIN RF ATTEN dB, and REFERENCE LEVEL selectors are rotary switches where each contact occupies a position in the keyboard switch matrix. The TIME/DIV and MIN RF ATTEN are position dependent. The master processor notes the current setting of these selectors by noting which contacts are closed. When a change is made the master microcomputer notes which direction the selector was moved by noting the relative position of the current contact closure with the previous setting. Pull-up resistors, within R2041 plus R2044,on each column of the row currently being read, will pull that column high if the switch is open. The basic algorithm of scanning is to pull one row at a time down and note which columns have a 1 or 0 . Port one, P10-P17, (pins 27-34) read the columns. Part of port two (pins 21-24) are responsible for activating the rows. Basically the process consists of pulling one row at a time down to a logic 0 and then reading all the columns. If a switch contact is open it reads a "1" and if it is closed it reads a "0".

Since there are 10 rows to scan and only 4 pins (P20-P23) available at the number 2 port, the output is multiplexed through U4021 and U5021. These IC's are open collector output, TTL compatible multiplexers. They decode data out of P20, P21, P22, and P23 (pins 21-24) and their output pulls the appropriate row of keys down. Figure 7-33 is a chart showing the switch matrix codes, and which keys correspond to a given address in the matrix code. Note that column 6 contains the MIN RF ATTEN settings, column 7 the SPAN/DIV and RESOLUTION BANDWIDTH settings, column 8 the REFERENCE LEVEL settings, and columns 1 & 2 are devoted entirely to the TIME/DIV selections.

Due to the characteristics of the switch matrix, if two keys, in any row or column are closed, and a third is closed so three corners of a rectangle are established in the key matrix, the CPU will see a phantom closure at the fourth corner. For example; if Y6/X3, Y6/X7 are closed, and then Y3/X7 is closed, the CPU will see a phantom closure at Y2/X3 as it scans the key matrix. To suppress these phantom key closures, diodes have been added in series with the RESOLUTION BANDWIDTH, MIN RF ATTEN, SPAN/DIV, and certain other keys in column 6 and 7 of the key matrix. In addition, an error detection algorithm is used in the CPU to eliminate additional phantom key closures that might occur.

Scanning the FREQUENCY Control Coder

The FREQUENCY control contains a pair of phototransistors that output a gray code through U1024B and U1024C to P27 and P26 (pins 37 & 38) of the CPU. This gray code signifies the direction the control is turned. During a scan cycle, the CPU looks at the status of the FREQUENCY control code and if it detects a change, the CPU performs a shift and exclusive-OR operation which derives the correct code to output over the instrument bus to the master processor to tell it which direction to tune the center frequency.

Outputting the Correct code

The remaining two bits out of port 2 (P24 and P25) drive the appropriate hardware and initiate an SRQ on the instrument bus. When the SER REQ line is pulled down, the master processor will service either the keyboard or the frequency coder. The front panel CPU (U3039) initiates a SRQ by pulling down P24 or P25. A low out of P24 (pin 35) will initiate a keyboard SRQ. The master processor will now service the request by reading the keyboard data in output buffer U4030. A low out of P25 (pin 36) initiates a FREQUENCY control SRQ and causes the master processor to service the request by reading the frequency code in the output buffer.

A low out of P24 is inverted by U2020C so it clocks the flip-flop U3013B. The resultant low on the $\overline{Q}$ output pulls the SER REQ line down.(Refer to the instrument bus POLL sequence described under the master processor description for the service request sequence.) The master processor now raises both the POLL line and AB7. This is gated through U4014A as a low to DB0 on the instrument bus. The master processor reads the bus and sees a low on DB0. This indicates that a keyboard interrupt has occured and it must read the new keyboard code. The master processor first clears the interrupt by pulling AB7 and then the POLL line low. DB0 now goes high. The processor now writes a 0 to DB0, the same as it read, and raises the POLL line. This clocks U3013A and resets U3013B which removes the $\overline{SRQ}$. The instrument processor now reads the data in the output buffer, U4030, at address F4. The front panel CPU now recognizes that its output buffer has been read and it resets P24 to a 1. It is now ready for another cycle.

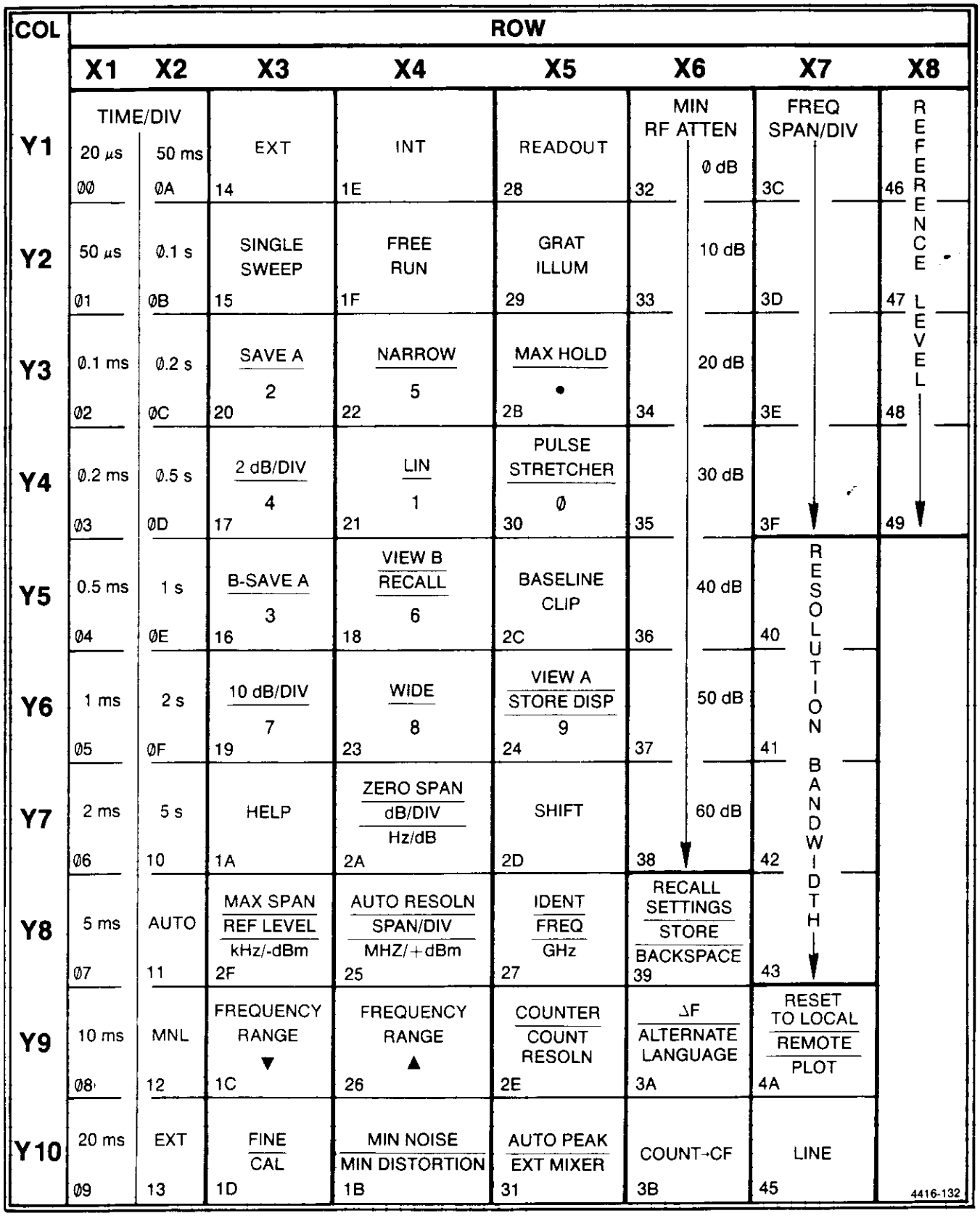


Figure 7-33. Front panel switch matrix code.

A similar process occurs when P25 (pin 36) of the CPU is pulled low by a FREQUENCY coder interrupt. A low on P25 is propogated through U2020B, U2013A, U2013B,and U4014C; only this time DB3 is involved in the poll. U2020A and U4014B decode a low on AB7 and high on POLL line to clock U2013A and 3013A.

Software

The algorithm that the CPU follows consists of a main scan routine, which is an endless loop, and four subroutines that can be called. One sub-routine runs the on-chip timer that is used to debounce the keys, another reads the frequency knob coder and derives the proper code to output to the master processor, the third subroutine reads the keyboard and stores the address of all keys that were closed, and the fourth subroutine looks at the keycode from the key addresses that were stored, and outputs the key codes and/or frequency code for the master processor. There are also a number of checks and tests that have to be done in each routine in addition to the obvious tasks.

Main Scan Routine

There are two types of scan; the first is made after a reset, the second type consists of the following scans; the keyboard, frequency coder, and the output data. During the first scan, data in the CPU is initialized. The CPU reserves part of its RAM to store and remember all key and frequency knob coder settings. During all scans, the CPU reads the frequency code and each row of keys on the keyboard. It compares what it read to that stored in RAM and if there is a difference, the CPU calls the appropriate subroutine for either the keyboard or the frequency coder knob. After a complete scan, the CPU checks to see if new information needs to be output to the instrument processor. If it does the CPU calls up the output subroutine.

Prior to the first scan, after reset, the CPU puts all 1's (highs) into its keyboard memory. This corresponds to open keys. On the first scan, the CPU will note five apparant closures due to the TIME/DIV, MIN RF ATTEN, SPAN/DIV, RESOLUTION BANDWDITH, and REFERENCE LEVEL selectors.These closures are noted and output to the master processor. Because the master processor memory knows the position of each selector to close a key, the processor calls these the power-up settings. When a front panel knob changes position the master processor can determine which direction the knob changed and what it must do to respond to the change. A complete scan, without detecting any key closures takes about 800 μs.

Keyboard Check Subroutine

This subroutine is called when the main scan routine detects a change in the keyboard matrix which occurs when a key opens or closes. A key opening usually signifies that an action has been completed, whereas a closure indicates that an operation or action is requested by the user; therefore, the two are treated differently by the CPU.

Because mechanical keys tend to bounce when they open or close, the subroutine must debounce each key change. To debounce, the subroutine calls up the timer subroutine. This sets a number into the internal timer and starts it running. When the timer has timed out, in about a millisecond, the keyboard subroutine again scans the row and compares this scan with the scan before the debounce check. If the scan does not compare, the routine assumes the key change was a bounce or fluke, and it returns to the main scan routine.If it does compare, the routine then recognizes that a key state has changed. It then checks to see if this is the first scan that looked for a key change after it has outputted previous information to the master processor. If it is the first pass then the routine causes the CPU to re-scan the full keyboard matrix to ensure that there is not a phantom key closure. If this is the second or subsequent pass and an actual key change has occured, the routine then notes if the key change was an opening or closure. If it was an opening the CPU memory is updated to the fact that the key is open. If a closure has occurred, the routine will then check the column that has the closure and output a new key address onto the output stack. This address consists of the key's row and column location. After outputting the address, the subroutine returns to scanning the remainder of the keybord matrix.

Frequency Coder Subroutine Check

This subroutine is called when the main scan routine detects a change in the frequency coder switch. Like the keyboard subroutine, this routine also debounces the frequency coder switch after every change to ensure that the switch code has changed. If a real change is noted, the routine proceeds to determine the direction of the change. The frequency knob outputs a two-bit code with only one bit at a time changing as the control is rotated. The direction the knob is rotated is determined by the property of a gray code, generated by an exclusive-OR logical operation within the CPU. The previous state of one bit is compared with the current state of the other bit. Down (counterclockwise roatation) yields unequal inputs, while up (clockwise rotation) yields the opposite. The bit that indicates direction is inserted as the MSB for the frequency coder byte. This byte is then loaded into the output stack . The subroutine then returns to the main scan routine.

Output Subroutine

After each scan, the CPU checks its output register to see if any information needs to be output. If it needs to be output,the output subroutine is called up; if not, another scan is started. The output subroutine checks a number of things before it outputs any information to the output regis-

ter. It first determines if the CPU is on its first or initial scan after a reset. The first scan will contain more than one closure. All of these closures must be output before it continues. On all scans that follow, the routine looks for more than one closure by checking the number of entries into the output stack. If more than one closure has been entered, the output routine aborts. This eliminates outputting phantom key closures.

The routine is now ready to output information. It pulls a key address from the output stack and looks up the code from a look-up table in ROM. This key code is loaded into the data port or output buffer. The appropriate port P24 or P25 (pins 35 & 36) is pulled low. The routine continuously reads the frequency coder and updates its memory while it is waiting for the master processor to read the data in the output buffer. Once the data has been read, P24 or P25 goes high and the subroutine starts to check the output stack for more key closures. When the output stack is empty, the first scan flag is rescinded and the CPU returns to its main scanning routine.

POWER SUPPLY

The Main Power Supply furnishes all the regulated voltages for the 494/494P, except the crt high-voltage supply. The high-efficiency design of the Main Power Supply reduces total weight and conserves energy. The power supply consists of the following: the line input circuit, which rectifies and filters the incoming line voltage; the inverter, which drives the primary of the power transformer; the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; and the regulator circuits, which control the voltage and current for the supplies that require precise regulation.

The Fan Driver board houses the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Over-Voltage Protection circuit, which shuts down the +5 V supply in case of over-voltage. Refer to Diagram 46.

Line Input Circuits

Power is applied through line filter FL301, line Fuse F301, and through FL302 (for additional normal mode/common mode EMI filtering) to POWER switch S300. The power is then sent through line selector connector J1091. The line filter prevents power-line interference from entering the power supply, and it also prevents internally-generated signals from radiating out the power cord.

Line selector switch S302 allows instrument operation from either a 115 V nominal or 230 V nominal line voltage source. With S302 is in the 115 V position, pins 1 and 2 of P1091 are connected to the input power, and rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. With S302 in the 230 V position, pins 2 and 3 of P1091 are connected to the input power and CR3096, CR4095, CR3098, and CR4094 operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

Thermistors RT2093 and RT2097 limit current surge at turn on. After the instrument warms up, the current demand drops. The increase in temperature decreases the resistance value of the thermistors so they have minimum affect on the circuit.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the POWER switch is turned off. A relaxation oscillator formed by C5113, R5111, and DS5112, indicates the presence of voltages in the circuit until the poten- tial across the filter capacitors is below 80 V.

Thermal cutout switch S2103 opens if the interior of the instrument reaches 103°C to prevent overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak voltage surge in excess of 230 V occurs across the input, or if the instrument is accidentally connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230 V, E1094 and E2095 operate in series to protect the input against line surges of approximately 460 V peak.

The voltage for the line trigger is taken across CR3096. This 48 Hz to 440 Hz voltage drives optical isolator U5043.

The pulsating 5 V output is ac coupled, then sent both to the Sweep circuit to provide instrument triggering at the line frequencies and to the Z-Axis board for the Power-Fail Detector circuit.

Inverter Circuit

The inverter consists of a multivibrator that produces a rectangular shaped signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control the duty cycle of the inverter driver and the inverter output stage. The primary regulator circuit compares the +17 V supply output with a reference voltage, then gates the inverter logic circuits off and on to control the inverter duty cycle and the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of main power transformer T4071. The primary over-current sense and soft start circuits add protection.

Multivibrator. U6059, a low-power 555 timer, is a multivibrator that operates at approximately 66 kHz and 90% duty cycle. Oscillator frequency is adjusted by R6061. The output rectangular shaped signal is applied through R6052 to the primary of T6044 in the ramp generator and also directly to U6053, U6063A, U6063B, and U6069.

Ramp Generator. The ramp generator circuit is a gated sawtooth generator that consists of T6044, Q5023, Q6034, Q5032, and related components. The negative excursion of the rectangular shaped signal from U6059 is coupled across T6044 to force Q6034 into conduction. This forward-biases Q5032. Its collector moves toward +17 V to charge C5038 to this value. Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Q5023 acts as a constant-current drain to linearly discharge C5038. This signal is coupled across divider R5036/R6032, then applied through C6039 to the input of comparator U6036, which is part of the primary regulator.

Primary Regulator. The primary regulator circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter. The +17 V is divided by R6038 and R6037 to approximately +4.8 V and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the non-inverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The non-inverting input receives a sawtooth signal of approximately 500 mV peak-to-peak superimposed on a +5 Vdc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Note in Figure 7-34 that as the level at pin 3 (which corresponds to the +17 V supply variations) rises and falls, the duty cycle of the output waveform varies accordingly.

The output signal of U6036 is applied to optical isolator U6043, which drives the input of U6069.

Inverter Logic. This stage consists of steering flip-flop U6063B and dual quad input NAND gate U6069. The flip-flop is connected so it toggles to enable first one gate then the other. The square-wave output from the multivibrator drives the clock input of U6063B. The signal also enables each gate to ready it for the other signals that arrive later. The output state of U6063 determines whether the upper or lower section of U6069 will be ready for the enabling signal. Assume that the Q output of U6063B is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gated pair disabled. When the output of U6043 moves high (U6043 controls the duty cycle of the inverter, the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, so the lower half of U6069 is enabled and Q6077 is now in the conduction path.

Inverter Driver. The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push-pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage. This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration. The two transistors drive the series tank, which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and it, in turn, drives the secondary circuits.

Primary regulation, as discussed previously, occurs when the duty cycle of the inverter driver main switching transistors is varied. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 10% of the period, or 1.5 μs. This short interval allows any stored base charge to deplete, so there is no chance both transistors will conduct at the same time. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for approximately 6 μs, or 40% of the total period.

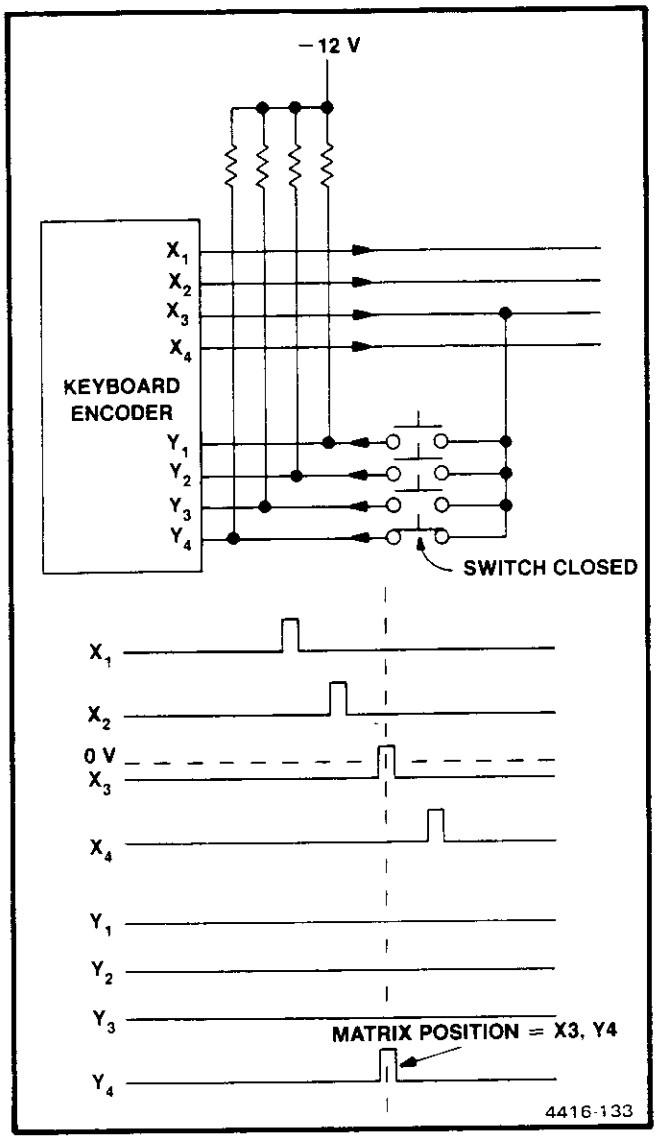


Figure 7-34. Primary regulator input/output waveform (stylized).

Soft Start and Primary Over-Current Circuits. The soft start circuit consists of U6053 and associated components. Soft start gradually increases the switching transistor's duty cycle at turn-on or after over-current shutdown to prevent excessive transistor current due to charging output capacitors. Refer to Figure 7-35 for timing waveforms.

The primary over-current circuit protects against secondary shorts that could destroy the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at approximately 6 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for approximately 1 sec and to reset the soft start circuit.

Rectifier-Filter Circuits (secondary section).

Transformer T4071 has three secondary windings. The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the −7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and −17 V supplies. The linear regulated supplies (+5 V reference, +5 V, −5 V, +15 V, and −15 V) derive their current from the rectifier-filter circuits.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3052, CR1042, CR1034, CR1022 and associated capacitors,compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062. The output is filtered and sent to the rest of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051 to become the +7 V and −7 V supplies. The +7 V supply is only used on the Main Power Supply board; the −7 V supply is used by other circuits in the instrument.

The third winding of T4071 (pins 13, 14, and 15) furnishes current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output is divided to become the +17 V and −17 V supplies. The −17 V supply is used only on the Main Power Supply board; the +17 V supply is used both on the Main Power Supply board and elsewhere in the instrument.

+5 V Voltage Reference Supply. The +17 V is divided down by a voltage divider to Zener diode VR6026. The 6.2 V from VR6026 is divided across R6029, R6028, and R6023. CR5031 provides a regulated source of bias to VR6026 after +15 V comes up.The +5 V REF adjustment, R6028, is set by monitoring the +15 V supply and setting it for a precise +15.00 V.

Regulator Circuits. The +15 V, −15 V, +5 V, and −5 V are regulated. Since all four regulators are basically the same, only the +5 V regulator is described. Significant differences are discussed following this description.

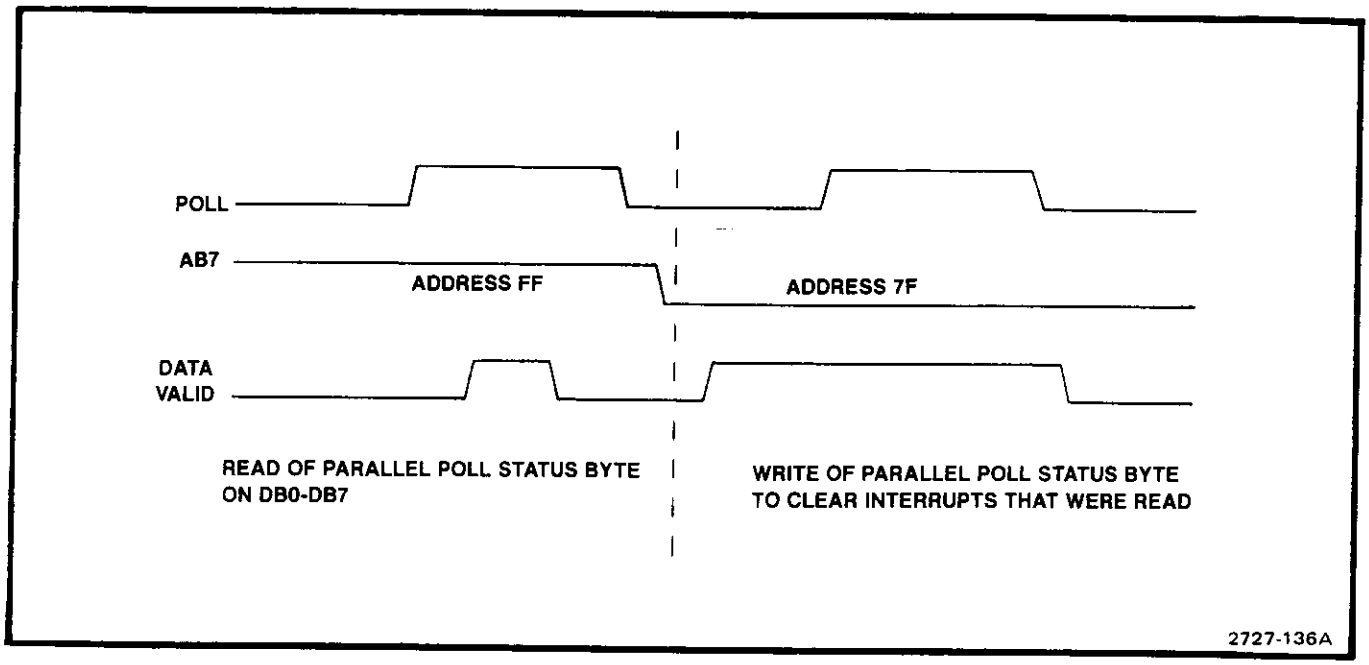


Figure 7-35. Timing waveform (stylized) for soft-start circuit.

U2037A, the voltage regulator part of the circuit, compares the +5 V_{REF} and +5 V SENSE voltages, amplifies the difference, and applies the change to driver transistor Q2023. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 to change its conduction and correct for the original change to the +5 V. The +5 V sense samples the +5 V at a distribution point on the Mother board. This signal compensates for voltage (IR) losses to that point.

U2037B is the current limiter portion of the regulator. The amplifier detects the voltage differential across the current sensing resistor R2017, which is in series with the output load. When the overload threshold is reached, as set by R2017, R2039, R3032, and R3031, U2037B removes bias current from driver transistor Q2023 and Q2024. The negative bias on R3031 allows the limiter to remain active under short circuit conditions.

The −15 V regulator is the same as the +5 V regulator, except that the current limiter, U2037D supplies additional positive bias for Q2031 when it is not active . The −15 V regulator is virtually identical to the +5 V regulator. The −5 V regulator differs from the others in that a driver stage is not required, so the preamplifiers drive series-pass transistor Q5013 directly.

+5 V Over-Voltage Protection Circuit. Zener diode VR1015 and SCR Q1010 form the over-voltage protection circuit. If the +5 V supply passes +6 V, the potential on the gate of Q1010 biases it into conduction. This forces the +5 V supply to ground; it remains at ground potential until the analyzer is de-energized and turned on again.

Fan Drive Circuit. The fan drive circuit provides a temperature-controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a voltage regulator controlled by thermistor RT2045. The value of RT2045 varies inversely with the internal temperature of the analyzer. The thermistor and a companion resistor, R2042, fix the turn-on voltage at the emitter of Q1044 at approximately −13 V; the voltage goes more positive as the analyzer warms up. VR 2038 is connected with jumper P2043 when the rackmount fan is used to prevent the output voltage from going below approximately 9 V.

The ring counter consists of three stages: Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020, with R2014/C2012 and R2016/C2018 as the frequency-determining components. When the analyzer is energized, one of the three ring counter stages begins to conduct before the

others; owing to circuit imbalances. Assume that the upper stage (Q1025 and Q1020) begins to conduct first. The collector voltage of Q1025 is near −17 V, which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. Operation of the other two stages is prevented until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit produces a three-phase drive signal of approximately 240 Hz. the inductance of the motor coils round off the otherwise sharp corners of the drive signal, so the current waveform looks a great deal like the output of a half-wave rectifier at P2020 pins 1, 2, and 3. Each drive signal is approximately 120° apart, so as to drive the motor.

The rackmount/benchtop versions of the 494/494P require an external fan, B200. When this fan is installed, the internal fan, B100, is removed.